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Diagnostics Manual

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Diagnostics Manual
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Revision Sheet

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Diagnostics Manual

Edition	Document No.	Date	Description
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Second, Rev. 1	760-000750-204	May 1989	Addendum containing updates to *io4000*, the Preface, and the addition of a new test, *dev5210*.
Second	760-000750-203	October 1988	This release contains minor updates to all of the diagnostics. Several of the tape and disk diagnostics contain major revisions.
First	760-000750-202	June 1988	First release. Contains all I/O and peripheral tests from the *C1 Diagnostics Reference Manual*.

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Preface

Purpose and Intended Audience

The *CONVEX PBUS I/O System Diagnostics Manual* is the third of four volumes in the *CONVEX Diagnostics Documentation C200 Series*. The other volumes include the following:

- *CONVEX Diagnostics Master Index (C200 Series)*
- *CONVEX Processor Diagnostics Manual (C200 Series)*
- *CONVEX Diagnostic Utilities Manual (C200 Series)*

This manual is divided into chapters that encompass the operation and interpretation of the various I/O system functional tests. This manual is not a tutorial, but rather a reference for the users of diagnostics, including field service and manufacturing test personnel, as well as the diagnostics sustaining staff. In addition, CONVEX customers can use this manual to execute diagnostics.

Scope

This manual applies to all CONVEX computers.

Outline

Each chapter in this manual covers a specific diagnostic function. To identify the general contents of each chapter, prefixes appear before the page number. The class and subtest descriptions and the invocation procedures of each test are covered within each chapter. The organization is as follows:

- **Diagnostics Environment** — Contains an introduction to the theories and concepts that underlie I/O diagnostics on CONVEX machines as well as the basic overview, philosophy, and structure of I/O diagnostics
- **EGOS Overview** — Provides a brief overview of the Event Governed Operating System (EGOS) and how it relates to device and peripheral diagnostics testing
- **Dshell Overview** — Provides a brief overview of and a general introduction to the *dshell* utility
- **io** — Describes the IOP/VIOP and channel control unit tests
- **dev** — Describes all peripheral tests
- **Appendix A** — Contains information concerning how to use the *contact* facility to report problems

Notational Conventions

The notational conventions used in this text are listed below:

- Bit numbering is left to right, `N-1` through `0`. The most significant numerical bit is `N-1`, the least significant `0`. The bit numbering represents the binary weight of a position.
- Bit fields are specified using the following convention: *name*<*x..y*> where the bit field is *name* from bits *x* through *y*.
- Individual bit positions within a register are denoted by specific positions separated by commas. For example, REG<15,4,0> denotes bits 15, 4, and 0 of REG.
- Byte numbering is from left to right
- A *bit* is a single binary value or entity
- A *nibble* is 4 bits
- A *byte* is 8 bits
- A *halfword* is 16 bits
- A *word* is 32 bits
- A *longword* is 64 bits
- *Single precision* is a 32-bit floating point word
- *Double precision* is a 64-bit floating point longword
- An *instruction* is a multihalfword operand
- A bit is *set* when it contains a binary value of `1`.
- A bit is *clear* when it contains a binary value of `0`.
- All memory and I/O addresses are written in hexadecimal notation unless explicitly stated otherwise.
- All register contents are written in hexadecimal notation unless explicitly stated otherwise.
- A *register* is a programmer-visible hardware storage element internal to the processor
- *Physical memory* is the physical storage installed in the processor
- *Virtual memory* is the perceived amount of physical memory as seen by the application programmer
- The symbol *K* is an abbreviation for *kilo* or 1,024
- The symbol *M* is an abbreviation for *mega* or 1,048,576
- The symbol *G* is an abbreviation for *giga* or 1,073,741,824
- TBD is an abbreviation for *To Be Determined*
- A *stack* is a linked-list group of words useful for dynamic allocation and deallocation of memory
- A *return block* is a collection of registers that is pushed or popped from a context stack in response to an instruction or other event
- *Reserved* or *undefined* convey what to expect, if anything, from unused fields in registers, reserved memory, or reserved I/O space. Algorithm implementation based on the use of undefined or reserved fields is not recommended.

Warnings

The following is an example of a warning and its typical content and location as used in CONVEX documents:

WARNING

Warnings highlight procedures or information necessary to avoid injury to personnel. A warning immediately precedes the critical information and includes a description of the hazard.

Cautions

The following is an example of a caution and its typical content and location as used in CONVEX documents:

CAUTION

Cautions highlight procedures or information necessary to avoid damage to equipment, loss of data, or invalid test results. A caution immediately precedes the critical information and includes a description of the possible damage.

Notes

The following is an example of a note and its typical content and location as used in CONVEX documents:

NOTE

A note highlights useful information that is supplemental in nature. A note may immediately precede or follow the information that is being highlighted.

Associated Documents

The following is a partial list of other manuals or books that may provide more detailed information on the topics presented in this manual:

- *CONVEX Processor Diagnostics Manual (C1, C120)*, Order No. DHW-071

- *CONVEX Processor Diagnostics Manual (C200 Series)*, Order No. DHW-081
- *CONVEX Architecture Reference*, Order No. DHW-005
- *CONVEX SPU UNIX Utilities Manual*, Order No. DHW-007
- *CONVEX Processor Operation Guide (C100 Series, C200 Series)*, Order No. DHW-015
- *CONVEX Diagnostic Utilities Manual (C1, C120)*, Order No. DHW-072
- *CONVEX Diagnostic Utilities Manual (C200 Series)*, Order No. DHW-082
- *CONVEX UNIX Tutorial Papers*, Order No. DSW-002
- *The C Programming Language*, Kernighan & Ritchie, Order No. DSW-046

Ordering Documentation

To order the most current version of this or any other CONVEX document, use the product number. If the product number is not known, order by the exact title. In some situations, the most current version may not be desired. To receive a specific version of a manual, order the manual by its document number, or part number, which can be obtained by contacting the local CONVEX office or by calling the Technical Assistance Center.

The product number for this manual is DHW-008.
The document number for this manual is 760-000730-000.

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- From locations in Alaska, Hawaii, and Canada, call 1(214)497-4379.
- From all other locations, contact the nearest CONVEX office.

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- The chapter and page number in question
- The comment

Reader's Forum

If you wish to mail your comments to us, please use the form at the end of this manual and list the document page number with your questions and comments. Thank you.

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David Massey, Lead Writer
CONVEX Hardware Documentation

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Chapter 1
Diagnostics Environment

1.1 Overview

CONVEX system diagnostics consist of a suite of test programs designed (except where noted) to execute under the Service Processor operating system, SPU UNIX. These programs utilize the capabilities of the Service Processor to test the operation of one or more of the functions of the system and report any errors detected. All of the diagnostics in this manual are intended to be executed "off-line"; that is, while CONVEX UNIX is not being executed by any of the Central Processing Units (CPUs) in the system.

The Service Processor, together with SPU UNIX, various diagnostic utilities, and the test programs, themselves, comprise the CONVEX diagnostic environment. This chapter describes the hardware and software components of this environment and is intended to provide the background necessary to fully utilize the capabilities of the CONVEX processor diagnostics.

For more information about the diagnostic environment refer to the Diagnostic Environment chapter in the *CONVEX Processor Diagnostics Manual (C200 Series)* or the *CONVEX Processor Diagnostics Manual (C1, C120)* depending on the architecture of the machine under test.

1.1.1 Test Program Naming Conventions

Test program names are in the form *cattypedevnn.suffix* where:

- *cat* is the subsystem being tested
- *type* is the type of test being performed, e.g., standalone, self-test, or offline functional test
- *dev* is the device being tested, e.g., disk, tape, or printer. This segment of the test program name is used *only* if the category is a device.
- *nn* is a CONVEX code used for distinguishing between test programs
- *suffix* is one of three program identifiers:
  - *.t* are programs that execute on SP2
  - *.x00* and *.rnn* are object files for different target processors other than the SP2. The target processor depends on the subject of the test. The test program name must have the test program category (*cat*) at the beginning of the name to determine the target processor.

1.1.1.1 Test Program Categories

Test program categories include those tests for the CPU, peripheral devices, I/O system, memory system, SP2, and entire system. For example, *cpu4041* is a CPU vector instruction test while *mem4000* is a memory system functional test. The following table lists test program categories:

Table 1–1, Test Program Categories

TEST PROGRAM CATEGORIES	
Test Category (*cat*)	**Description**
cpu	CPU subsystem related test
dev	Peripheral device test
io, idc	I/O subsystem related test
mem	Memory subsystem related test
spu	SP2 subsystem related test

1.1.1.2 Test Program Types

A test program type describes whether a test is a standalone test, self-test, kernel hardware test, or an offline or online functional test. See the following table for the numbering system and description of test program types:

Table 1–2, Test Program Types

TEST PROGRAM TYPES	
Number (*type*)	**Description**
0	Standalone test
1	Self-test
2	Kernel hardware test
4, 5	Offline functional test

1.1.1.3 Test Program Device Types

Test programs will test disks, tapes, terminals, printers, and networks. See the following table for the numbering scheme and a description of the test program device types:

Table 1–3, Test Program Device Types

TEST PROGRAM DEVICE TYPES	
Number (*dev*)	**Description**
1	Disk
2	Tape
3	Terminal
4	Printer
5	Network

1.1.1.4 Examples of Test Program Names

The following table presents some examples using the naming conventions outlined above:

> **NOTE**
>
> In the following table, SOFF stands for Standard Object File Format.

Table 1–4, Example Test Program Names

EXAMPLE TEST PROGRAM NAMES	
Test Program Name	**Description**
cpu4041.t	SP2 object code in *b.out* format for *cpu4041*
cpu4041.rnn	C210 or C220 machine object code in SOFF format (relocatable)
cpu4041.x00	C210 or C220 machine object code in SOFF format (linked to run in segment 0)
mem4000.t	SP2 object code in *b.out* format for *mem4000*
mem4000.x00	C210 or C220 machine object code in SOFF format (linked to run in segment 0)
dev4100.t	SP2 object code in *b.out* format for *dev4100*
dev4100.x00	IOP object code in *b.out* format

1.1.1.5 Current PBUS I/O System Test Program Name Assignments

See the following table for current PBUS I/O System test program name assignments:

Table 1–5, Test Program Name Assignments

TEST PROGRAM NAME ASSIGNMENTS	
Program Name	**Test Name**
dev4100	Multibus SMD Disk Test
dev4110	Multibus SMD Disk Formatter, and Interactive Test
dev4200	Multibus STC Tape Unit Test
dev4300	Multibus Terminal Controller Test
dev4400	Multibus Line Printer Test
dev4410	Multibus Plotter Functional Test
dev4500	Multibus Ethernet Controller Test
dev4510	Multibus HYPERchannel Controller Test
dev4540	Multibus X.25 Controller Test
dev4600	Multibus Emulator Controller Test
dev5130	VMEbus SMD/ESDI Disk Test and Formatter
dev5210	VMEbus STC Tape Unit Controller Test
dev5300	VMEbus Asynce Controller Test
dev5500	VMEbus Ethernet Controller Test
dev_ultra	VMEbus UltraNet Controller Test
io1000	EPROM-Based IOP Self-Test
io1200	VIOP Self-Test
io4000	Multibus I/O Subsystem Test
io4120	HSP/HIA Subsystem Test
io5000	VMEbus I/O Processor Test

Chapter 2
EGOS Overview

2.1 Overview

This chapter provides an overview of the Event Governed Operating System (EGOS) and how it relates to device and peripheral diagnostics testing. There are three basic types of EGOS systems, one for each type of CCU. There is one for the Multibus interface, one for the VME interface, and one for the HIA interface. This chapter will explain the three types of EGOS systems and how EGOS is positioned within the overall operating system environment.

2.2 Purpose of EGOS for Diagnostic Testing

EGOS is basically a simple operating system that the device tests use to handle interrupts, schedule processes, and generally allocate and control IOP/VIOP resources. The diagnostics code uses both EGOS and the Message Based System (MBS) to manipulate test program control over to the CCU side of the test program. MBS is not a part of EGOS but rather a system that allows a common section of memory to be used as a message area between multiple processors. For more information on MBS, refer to the *CONVEX Guide to Writing Device Drivers.*

EGOS initially sets up interrupt tables, determines how many chassis there are, and initializes its windows and resource allocation tables.

2.3 EGOS for the Multibus Interface

EGOS for the Multibus interface supports event driven device drivers. The Multibus version of EGOS takes interrupts that are local to a CCU and channels those errors to the proper piece of code to handle the error. It basically supplies the error interrupt handlers for the CCU error interrupts. It also contains support routines to control allocation of the various CCU-related resources.

2.4 EGOS for HSP Interface, HSP EGOS

EGOS for the HSP interface supports event driven device drivers. The HSP version of EGOS is like the Multibus version. It takes interrupts that are local to a CCU and channels those errors to the proper piece of code to handle the error. It basically supplies the error interrupt handlers for the CCU error interrupts. It also contains support routines to control allocation of the various CCU-related resources.

2.5 EGOS for VME Interface, VIOP EGOS

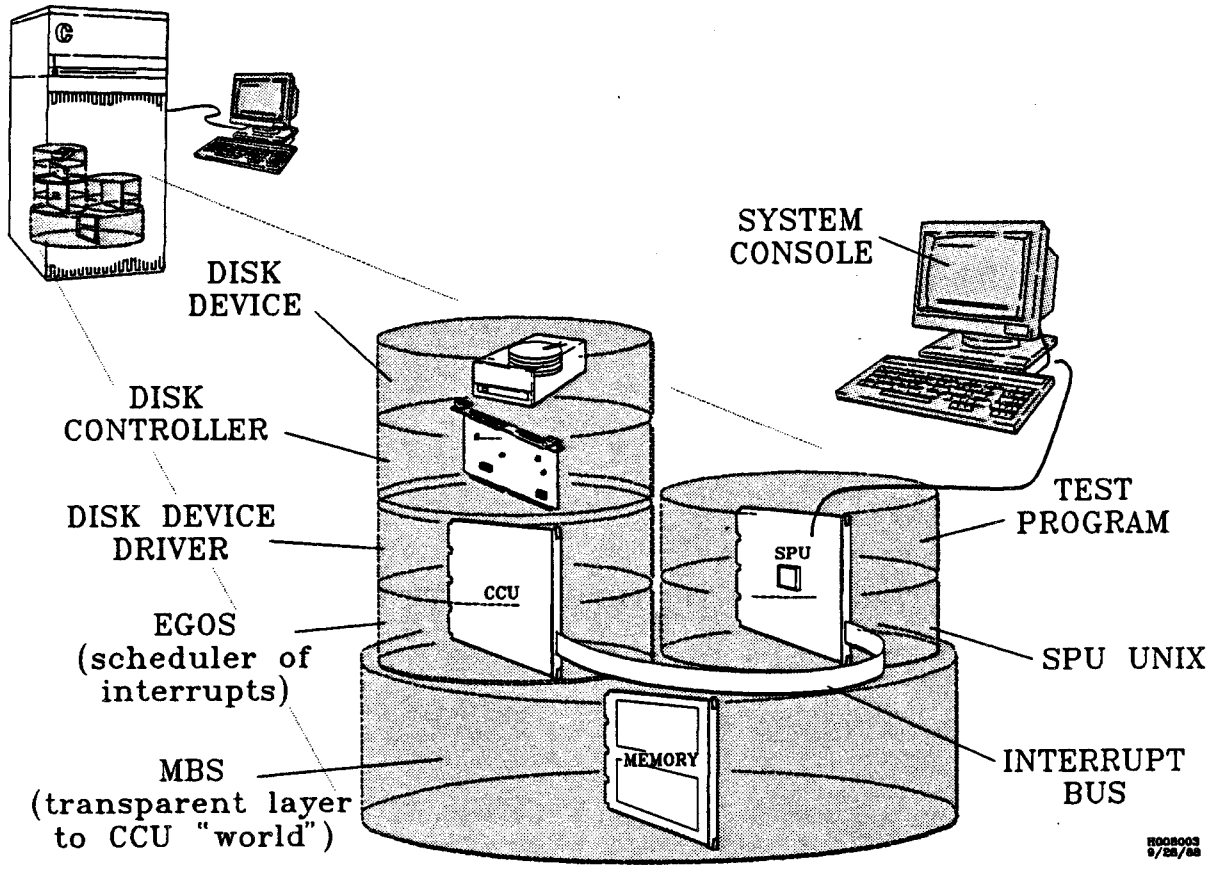
The VME interface version of EGOS is designed with a scheduler for the VIOP and is called VIOP EGOS. VIOP EGOS supports event driven device drivers as well as process type device drivers. VIOP EGOS utilizes a *sleep/wakeup* type of process control that improves efficiency of the device driver and makes it less complicated to create user written device drivers. Each process device driver has a priority level that can be defined relative to other processes. The scheduler supports 32 process priorities and is preemptive for higher priority processes. The VIOP hardware supports 14 device events for event driven device drivers. The 14 levels actually share 2 68020 interrupt levels. Therefore, two is the maximum number of processes at any given time.

2.6 EGOS Position in the Environment

EGOS is positioned in the operating environment between the actual device driver and MBS. MBS is a transparent layer that bridges the CCU and its resources to SPU UNIX. SPU UNIX handles many of the message manipulations that occur during testing. Many error messages that occur during diagnostics testing come from the device driver. When the device driver detects an error from the controller, it calls a routine in EGOS that places a message in the MBS system. This causes SPU UNIX to be interrupted and it retrieves the message from MBS. SPU UNIX then passes a signal to the test program. The test program then prints an error message to the console based on the code that it received.

The following figure illustrates the position of EGOS in the operating system environment.

Figure 2–1, EGOS' Position in the Environment



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Chapter 3
Dshell Overview

3.1 Overview

This chapter provides a brief overview of the *dshell* utility. Included in this overview is an overall explanation of the utility and a list of the utility's commands. For a complete description of this utility, refer to the Dshell chapter of the *CONVEX Diagnostic Utilities Manual (C200 Series)* or the *CONVEX Diagnostic Utilities Manual (C1, C120)* depending on the architecture of the machine under test.

3.2 Diagnostic Shell (*dshell*) Overview

The Diagnostic Shell (*dshell*) is a command interface program that runs on the Service Processor. Most of the diagnostics available for the CONVEX machines are interfaced through the *dshell*. Certain peripheral diagnostics are run as standalone tests. To determine whether a test can be run under the *dshell*, consult the appropriate chapter in this manual.

The *dshell* has two basic functions:

- Selecting diagnostics for execution
- Selecting test options
  - Pause on a failure or at the beginning or end of any specific subtest
  - Loop on a specific type of subtest or on a given set of subtests
  - Select subtest execution order
  - Direct test output to a file or to the screen (or both) to monitor the test as it runs or to analyze test results later
  - Select long or short error messages, or turn messages off
  - Execute either user-created or predefined command scripts

The following table list the various *dshell* commands and their functions.

Table 3–1, *dshell* Commands

COMMAND	FUNCTION
! [command]	This command is used to access, or *fork* a UNIX shell to execute the command that follows *!*.
exit	The *exit* command causes immediate termination of the *dshell* process and any test processes that may have been forked.
quit	The *quit* command causes immediate termination of the *dshell* process and any test processes that may have been forked.
^C	Returns user to the *dshell* command level if no subtest is running.
^B	Immediately terminate the *dshell* and any associated active processes. Core is dumped.
help	The *help* command causes a standard *help* menu to be displayed. The menu describes the correct command syntax for each *dshell* command and gives a terse description of what each command does.
status	The *status* command generates a report on the current state of the *dshell* command options. This report gives the name of each flag, its current value, and an explanation of its current effect.
log [options]	The *log* command provides a mechanism for specifying the number of failures that will be allowed to occur before a test or subtest terminates execution.
loop [options]	The *loop* command causes the *dshell* to repeat the execution of a test or subtest.
msgs [options]	The *msgs* command enables or disables different levels of test, class, and subtest result messages.
pause [options]	The *pause* command returns program control to the *dshell* to the beginning, end, or failure of all or specific subtests.
test [options]	The *test* executes specific tests, and displays test, class, and subtest menus.

3.3 Syntax Help for *dshell* Commands

The syntax for each *dshell* command can be obtained by typing the command with no options and pressing <**CR**>. For example, by entering **loop** and pressing <**CR**>, the syntax help in the following figure will be displayed on the screen:

Figure 3–1, Syntax Help for the *loop* Command

```
: loop
Proper syntax is:

loop off (-s) (-t)                          :disables loop modes
loop -s nnn                                 :loop on subtest nnn
loop -t                                     :loop on test
```

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io4000

Multibus I/O Subsystem Test

Overview

The *io4000* test verifies the functionality of a specified Input Output Processor (IOP). The *io4000* test verifies the following on the IOP(s) specified:

- The 68000 on the IOP can correctly execute instructions
- The IOP local memory is functional
- The memory protection registers are operational
- The cache memory can be written to and read from, and the associated cache control bits are functional
- The four Multibus interfaces operate in loopback mode
- The IOP can boot a program from memory
- The voltages on all installed Multibus chassis are within tolerance

The functional test uses main memory as a communication port from the Service Processor Unit (SPU) to or from the IOP(s) being tested.

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test:

Table io4000–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
IOP	IOP
MBCU	MBCU
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Test Invocation

The *io4000* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *io4000* test, use the procedure shown in the following figure:

Figure io4000–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test io4000 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Entering only **test io4000** executes all *io4000* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure io4000–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test io4000 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )):

Figure io4000–3, Test Parameter Menu

```
                        ENTER TEST PARAMETERS

                []      Encloses allowed input ranges or values
                ()      Encloses the default value
                ^       Returns to the previous prompt
                :nn     Returns to the prompt # nn
                :       Returns to the first unsatisfied prompt
                :?      Reviews previous entries

1: Enter IOP numbers [34567][1]                          (5) ->
2: Do you wish to run the multibus voltage tests?
   [y,n]                                                 (n) ->
3: Enter OK, or :NN to return to question NN [OK]
                                                        (OK) ->
```

[1] The available selections for this prompt will vary depending on the machine architecture.

The prompts and responses appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience. The Test Parameter Menu illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example Test Parameter Menu, as the questions illustrated are examples only.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn -- Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

A description of the meaning of each prompt follows:

```
Enter IOP numbers [34567]                          (5) ->
```

This prompt allows for the selection of the IOP(s) to be scanned. (For more than one IOP, enter the numbers contiguously, for example 345.) After entering the IOP number(s), each IOP entered is scanned to see if it exists. Any invalid number causes the test to reprompt for valid IOP(s). The test executes only when all entries are valid.

```
Do you wish to run the multibus voltage tests?
[y,n]                                          (n) ->
```

This prompt selects whether Subtest 600, Multibus Voltage Test should be executed. If the default is selected, the multibus voltage test does not execute.

```
Enter OK, or :NN to return to question NN [OK]
                                               (OK) ->
```

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- Signals and interrupts for hard and soft errors are set
- Determine which Multibusses are present
- Determine whether the IOPs can run cache accelerated mode
- SPU local test variables are initialized
- The SPU verifies that the selected VIOPs are installed by scanning patterns into the VIOP LED register

After all the above events have occurred, the test code is started.

Class Descriptions

The *io4000* test contains the following four classes of subtests as shown in the following table. The individual class descriptions that follow list the time required to execute each subtest.

> **NOTE**
>
> The subtest execution times shown in this test description were executed at 10 Mhz on a system with one IOP and 16 Mbytes of main memory. The execution times are approximate and depend on factors such as memory size and number of IOP(s) under test.

Table io4000–2, *io4000* Test Classes

Class	Description
1	68000 subsystem tests
2	RAM pattern tests
3	Cache functionality tests
6	Multibus tests

NOTE

The first time one of the subtests in the 200–600 range is executed, the IOP(s) under test must be loaded with the test program, which adds about 20 seconds to the test times.

Class 1 Subtests

Class 1 subtests verify that the IOP can correctly load a program from main memory. These tests communicate with the SPU via the IOP LED register. The SPU places a command on the LEDs through the IOP scan ring. The IOP then reads the LED register, executes the specified command, and places the result in the LED register.

In general, a return code of zero indicates the test completed without error. When the test fails, a nonzero value is returned, which identifies the step in the subtest that failed. The SPU reads this code and prints the appropriate diagnostic message. Class 1 subtests are listed in the following table:

NOTE

The subtest execution times shown in this section were executed at 10 Mhz on a system with one IOP and 16 Mbytes of main memory. The execution times are approximate and depend on factors such as memory size and number of IOP(s) under test.

Table io4000–3, Class 1 Subtests

Subtest	Description	Time (min:sec)
100	IOP Reset	:02
101	IOP Self-test	:40
102	IOP Initialization Command	:01
103	IOP Boot Command	:02

NOTE

Subtest 100 must be run before subtests 101, 102, and 103. Also, subtest 103 cannot be looped.

Subtest 100, IOP Reset

Subtest 100 resets all the IOPs being tested.

> **NOTE**
>
> This subtest must be executed before subtests 101, 102, or 103.

Each IOP then performs the following:

- Tests operation of the instructions:
  - beq
  - bne
  - move <ea>,cc
  - cmpi #<data>,<ea> for all operand lengths
  - cmpa <ea>,an
  - cmp<ea>,dn
- Tests uniqueness of registers a0, d0-d1
- Tests functionality of all bits in a0, d0-d1
- Tests ability to calculate a checksum

If all of the previously listed tests pass, then the IOP performs a checksum test on the EPROM. If the checksum test passes, the IOP then enters a loop waiting for commands from the SPU to be passed through the IOP scan ring. If any of the above tests fail, an error signal is sent back to the SPU via the send-error bit in the miscellaneous diagnostic register, and the IOP 68000 performs a double-bus fault and dies.

Subtest 101, IOP Self-test

Subtest 101 places a self-test command on the red LEDs of the IOPs under test. Each IOP being tested then performs a series of seven tests (CPU2, RAM1, CPU3, RAM2, MAPTST, CACHETST, and MBLBTST). The following are descriptions of the tests:

CPU2

This test checks register functionality for the various 68000 registers, checks the addressing modes, verifies the jump and branch instructions, performs integer arithmetic tests, data movement operations, shift and rotate instructions, and bit-manipulation operations.

RAM1

This test determines the size of local memory by writing to the first word in each bank until a bus error occurs. It then performs a walking '1's and '0's test on the first word after the ROM and on the first word of all the following banks. Then, on the last 4 Kbytes of installed local memory, it performs a uniqueness test and a true/complement pattern test. Memory parity is checked by writing a word with inverted parity and then reading it to generate a parity error. The word is then rewritten with the correct parity.

CPU3

This test checks the 68000 instructions not tested in subtest 100 or CPU2 by using the

last 4 Kbytes of installed local memory as a stack. It also checks privilege violations and address errors. The *stop*, *trace*, and *reset* instructions are not checked.

RAM2

This test is similar to RAM1 except that it checks local memory from immediately after the ROM to the word preceding the last 4 Kbytes of installed local memory. A parity test is not performed.

MAPTST

This test performs a walking '1's and '0's test on the memory protection register at `0xff8000`. Then, it performs a uniqueness test and a true/complement pattern test for all the 256 registers. Next, it copies ROM to local memory and modifies the protection for installed local memory to valid, read, write, and execute. It clears the registers for uninstalled local memory. Then, memory protection is turned on, and the valid, read, write, and execute bits are verified from supervisor and user state. Finally, at the end of the test, memory protection is again disabled.

CACHETST

This test clears the cache after disabling cache parity checking and clearing the longword or byte dirty flags and the tag flag registers. Then, it reclears the tag flag registers and enables cache parity checking. Any pending cache or PBUS interrupts are cleared, and cache interrupts are enabled. The local memory copy of the EPROM is mapped in, and a checksum is performed on it. Next, the test sets the map registers to point to the last Mbyte of the PBUS. A unique pattern is written to the first 64 shortwords in each main memory 4 Kbytes window. As each word is written, the dirty bits are checked to see that they are updated appropriately. The test then clears the longword or byte dirty flags and marks all tag registers as loaded. Finally, the pattern written to each cache location is verified.

MBLBTST

This test resets the Multibus cable drivers and places them in loopback mode. In each Multibus window, the local memory copy of the EPROM is mapped in, and a checksum test is performed. The pattern left by the cache test is then checked through each of the Multibus windows.

Subtest 102, IOP Initialization Command

Subtest 102 determines the size of the installed local memory, and then clears local memory from the word following the EPROM to the end. The test then disables cache parity checking, and for each of the map registers performs the following:

- Clears the dirty 'a' and 'b' bits
- Clears the corresponding 128 cache bytes
- Clears the dirty 'a' and 'b' bits again

Next, the test enables cache parity checking, and points the first map register to the population configuration map on the MCU. The Population Configuration Map (PCM) is searched in order to locate the first 2 Mbytes of main memory. Once located, the map registers are initialized to

point to the first half of this 2 Mbyte block. The motherboard slot number is used to index into a table in main memory. This table contains a pattern, previously initialized by the SPU, that is to be echoed by the IOP. The pattern is the current time, in seconds, logically 'anded' with a mask of `0xffffff00`. When the IOP echoes this pattern, the subtest ends.

Subtest 103, IOP Boot Command

> **NOTE**
>
> Before executing Subtest 103, Subtest 102 must have completed successfully. This subtest checks only the SPU *load* command. Also, it is not possible to loop on this subtest.

Initially, Subtest 103 determines the size of local memory, and copies the EPROM to the last 16 Kbytes of installed local memory. A checksum is performed on local memory to verify it. The test sets memory protection for installed local memory to valid, read, write, and execute. The memory protection registers for uninstalled local memory are cleared. The interrupt status register is then cleared, and the IOP jumps to the local memory copy of the EPROM. Memory protection is enabled. The IOP slot number is used as an index into a table in main memory. The table is located in the first Mbyte of installed main memory.

After the test begins, the IOP enters a loop while waiting for the SPU to place commands in main memory. The valid commands are listed in the following table:

Table io4000–4, Valid SPU Commands for Subtest 103

Command	Description
load	Copies main memory to IOP memory, a byte at a time. As each byte is moved, *load* tallies it into a checksum. After main memory is moved, it checks for parity errors. If no errors, the checksum is placed in main memory; otherwise, negation of calculated checksum goes in main memory. At completion, *load* waits for more commands.
reset	Simulates a reset by loading the supervisor-stack pointer from memory location 0 and the *pc* from memory location 4.
jump	Jumps to the address specified in main memory. The *ssp* is set to the top of installed local memory.

Class 2 Subtests

Class 2 subtests are listed in the following table:

NOTE

The subtest execution times shown in this section were executed at 10 Mhz on a system with one IOP and 16 Mbytes of main memory. The execution times are approximate and depend on factors such as memory size and number of IOP(s) under test.

Table io4000–5, Class 2 Subtests

Subtest	Description	Time (min:sec)
200	PBUS Interrupt	0:09
201	PBUS Test-and-set	0:01
202	IOP Memory Access	0:01

Subtest 200, PBUS Interrupt

Subtest 200 verifies the ability of the IOP to request and use the PBUS interrupt bus. The subtest consists of the following three steps:

Step 1: Interrupt Receive Test

In the receive test, all 256 PBUS interrupts are sent by the SPU to the IOP, one at a time. After each interrupt is sent, the IOP verifies that only one interrupt was received and that the interrupt was received by the proper group. The group is determined by taking the modulo 4 residue of the interrupt number.

Step 2: Interrupt Transmit Test

In the interrupt transmit test, the IOP sends the SPU interrupt numbers 8, 9, 10, and 11 (the four interrupts that the SPU is capable of receiving). The IOP verifies that the acknowledge for each interrupt is received and the SPU verifies the reception of the four interrupts.

Step 3: Interrupt Loopback Test

The interrupt loopback test causes all 256 interrupts to be sent and received by the IOP in each of the four possible groups. Like the receive test, as each interrupt is sent, the IOP verifies that only one interrupt is received and that the acknowledge is also received.

NOTE

The terms receive and transmit are from the IOP's aspect.

Subtest 201, PBUS Test-and-set

Subtest 201 verifies that all PMAP registers operate in test-and-set mode by placing each PMAP register in test-and-set mode in sequence. The PMAP register that logically follows the register under test is prepared for non test-and-set operation and it verifies the operation.

A byte in the main memory command table is set to zero through the check window. It is read through the test window and the value returned is checked for a zero. The check window reads the byte in main memory and the value read is expected to be `0xff`. A second access through the test window verifies that the returned value is also `0xff`.

Subtest 202, IOP Memory Access

Subtest 202 verifies the IOP's ability to access all of allocated main memory. The test determines which blocks in memory are allocated by reading the PCM on the SPU, memory is allocated in 2 Mbyte blocks. The test writes and then reads a single unique integer value in each allocated block, and the test then re-reads each of the blocks to verify proper addressing.

Class 3 Subtests

Class 3 subtests verify the functionality of the IOP cache memory. The current subtests verify the cache in accelerated mode, normal mode, and in bypass mode.

> **NOTE**
>
> Not all of the subtests in Class 3 are currently implemented. Only the subtests that are currently available are listed in the following table.

Table io4000–6, Class 3 Subtests

Subtest	Description	Time (minsec)
300	IOP Cache Accelerate Read	2:26
301	IOP Cache Accelerate Write	3:42
302	IOP Cache Bypass Read	3:38
303	IOP Cache Bypass Write	3:36

> **NOTE**
>
> The subtest execution times shown in this section were executed at 10 Mhz on a system with one IOP and 16 Mbytes of main memory. The execution times are approximate and depend on factors such as memory size and number of IOP(s) under test.

Subtest 300, IOP Cache Accelerate Read

First subtest 300 sets the accelerate bit in the PMAP register. Then it sets the PMAP register that logically follows the window under test to nonaccelerate, nonbypass mode.

The IOP slot number is used to index into a table in main memory that contains patterns and pointers to main memory, which are used to test the accelerate function. The SPU initializes the table before the accelerate test command is given to the IOP(s). The table is accessed through the nonaccelerated PMAP register as described in the previous paragraph. The table has checksums and an IOP ID that are checked to ensure the integrity of the data.

Using the information from the table, the test checks the PMAP window under test. Before any location in the page under test is referenced, an initial 64-byte pattern corresponding to buffer locations `0` to `3f` is initialized to a known pattern through the nonaccelerated window. The pattern used for the first byte in the page is the IOP slot number plus the page number of the page under test, modulo 256. The test initializes each successive byte to the value of the previous byte plus 1, modulo 256.

Then a loop is entered in which each of the 4096 bytes in the page is read and checked for valid data. Additionally, each time byte `0` of each of the two cache buffers is read, the PTAG register for the page is checked to ensure the following:

- The accelerate-on reference bit is set.
- The loaded bit is set.
- The buffer dirty bit is clear.
- The TAG value and its parity are properly set.

Then, if the previous conditions are met, the test uses the nonaccelerated window to negate the current pattern in main memory. The original pattern remains in the cache. The pattern for the next 64-byte group then is initialized through the nonaccelerated window. When byte `1` of a buffer is read, the test checks the following:

- The accelerate-on reference bit is clear.
- The loaded bit is set for both buffers.
- The TAG value for the current buffer has not changed, and the TAG value for the other buffer is properly set.

Subtest 301, IOP Cache Accelerate Write

Subtest 301 initializes the main memory area used for the write test to the negation of the pattern to be written there. The test then uses the sum of the IOP slot number plus the page number of the page under test, modulo 256, as the pattern for the first byte. Next, it enters a loop into which each of the 4096 bytes in the page is written, one byte at a time. As each byte is written, the dirty bits for that longword are checked to make sure that they are set to the expected value. The test then checks the PTAG register for valid data. When byte `0x3f` of each buffer is written, the corresponding area of main memory is read through the nonaccelerated window to ensure that the pattern has *not* yet been written.

Every time byte `0` of a cache buffer is written, beginning with byte `0x40` in the page under test, the PTAG register is checked to verify that the accelerate-on reference bit is set. When byte `1` of a buffer is written, the nonaccelerated window reads main memory to verify that the pattern for

the previous 64-byte block is written to memory and to verify that the accelerate-on reference bit resets.

After the last 64-byte block is written, the window under test is flushed so that all data is written to memory. Finally, the test again checks the pattern in the entire 4096-byte block for integrity through the nonaccelerated window.

Subtest 302, IOP Cache Bypass Read

Subtest 302 tests each of the windows in the IOP cache. As in the accelerate read test, this test places the window that logically follows the window under test in nonaccelerate, nonbypass mode and verifies the operation of the window under test. Then it initializes the main memory area for the bypass test to the negation of the pattern to be written there. It uses the same patterns as those listed for Subtest 300, IOP Cache Accelerate Read Test.

For each of the 4096 bytes in the window, the test first uses the nonaccelerate window to write a one byte pattern to main memory. Then it reads the byte just written through the window under test and verifies the data. Finally it negates the byte in main memory through the nonbypass window.

Subtest 303, IOP Cache Bypass Write

Subtest 303 , the logical complement of Subtest 302, tests each window in the IOP cache. It initializes the main memory area used to test the cache to the negation of the pattern that is to be written there. It uses the same pattern described in Subtest 301, IOP Cache Accelerate Write Test.

For each of the 4096 bytes in the window, the test first uses the window under test to write a 1-byte pattern to main memory. Then it uses the nonbypassed window to verify that the pattern was written to main memory.

Class 6 Subtests

Class 6 subtests test the operation of portions of the Multibus Control Units (MBCUs) that are installed on the IOP(s) being tested. The system I/O configuration file, */ioconfig*, is read to determine what MBCUs are present.

> **NOTE**
>
> Not all of the subtests in this class are currently implemented. The subtest that is currently available is listed in the following table.

Table io4000–7, Class 6 Subtest

Subtest	Description	Time (min:sec)
600	Multibus Voltages	:01

NOTE

The subtest execution times shown in this section were executed at 10 Mhz on a system with one IOP and 16 Mbytes of main memory. The execution times are approximate and depend on factors such as memory size and number of IOP(s) under test.

Subtest 600, Multibus Voltages

Subtest 600 reads and tests the four voltages of each Multibus that is present for out-of-tolerance conditions. The voltages and tolerances for a Multibus are listed in the following table:

Table io4000–8, Multibus Voltages and Tolerances

Voltage	Minimum	Tolerance
+12.10	+11.40	+12.60
+05.10	+04.75	+05.25
-05.10	-05.75	-04.75
-12.10	-12.60	-11.40

io4120

HSP/HIA Subsystem Test

Overview

The *io4120* test verifies the operation of a High-Speed Parallel (HSP) Channel Control Unit (CCU) and HSP Interface Adapter (HIA).

The *io4120* test verifies the following local to the HSP:

- 68000 instruction execution
- HSP local memory operations
- HSP local memory protection
- Input bus integrity
- PBUS header generation
- PBUS access verification
- PBUS interrupt operations
- Correct HSP Address Translation Unit (ATU) operations in both physical and virtual address modes
- ATU error detection
- Output bus integrity
- Error status register verification

Additionally, the *io4120* test checks these functions that require the HIA:

- Register accesses
- Interface interrupt test
- Interface parity generation or detection
- Synchronous data transfers in both physical and logical address modes
- Bus arbitration
- Clock selection
- Channel interleave
- Error detection and recovery

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test:

Table io4120–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
HIA	HIA
HSP	HSP
FSE	FSE
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Test Invocation

The *io4120* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *io4120* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure io4120–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test io4120 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of the *CONVEX PBUS I/O System Diagnostics Manual*, for more information.

Entering only **test io4120** executes all *io4120* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of the *CONVEX PBUS I/O System Diagnostics Manual*. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases:

Figure io4120–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test io4000 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Example Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

Figure io4120–3 illustrates *all* questions that can be displayed during test parameter input.

Figure io4120–3, Example Test Parameter Menu

```
                              ENTER TEST PARAMETERS

                  []      Encloses allowed input ranges or values
                  ()      Encloses the default value
                  ^       Returns to the previous prompt
                  :nn     Returns to the prompt # nn
                  :       Returns to the first unsatisfied prompt
                  :?      Reviews previous entries

Hsp ccu slot number [0-3]                          (2) ->
Hsp default clock rate [0-3]                       (0) ->
Hia outclk default rate [0-3]                      (0) ->
Hia busclk default rate [0-1]                      (0) ->
Channel mask for compliance test - ls bit is chnl 0
[0x0-0xffff]                                  (0xffff) ->
Default power margin for HIA chassis (+5 only)
[l,n,u]                                            (n) ->
ATU scheme to test ('1' for C1, '2' for C2, 'b' for both)
[1,2,b]                                            (b) ->
Enter OK, or :NN to return to question NN [OK]
                                                  (OK) ->
```

However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example "Example Test Parameter Menu," as the questions illustrated are examples only.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

Each prompt is repeated and explained in the following paragraphs.

NOTE

The CCU slot specified is checked via the diagnostic bus to ensure that the HSP is present. Any invalid entry reprompts for the HSP slot number.

```
Hsp ccu slot number [0-3]                    (2) ->
```

Enter the CCU slot number the HSP resides in.

```
Hsp default clock rate [0-3]                 (0) ->
```

Enter the HSP default clock rate which sets the transfer rate from the HSP to the HIA. Enter **0** to select the highest rate.

```
Hia outclk default rate [0-3]                (0) ->
```

Enter the HIA outclock default rate which sets the transfer rate from the HIA to the HSP. Enter **0** to select the highest rate.

```
Hia busclk default rate [0-1]                (0) ->
```

Enter **0** or RETURN to select the default 40-MHz crystal. This crystal produces a 10-MHz transfer rate. Enter **1** to select a user defined crystal. A user-defined crystal, for example 1 36-MHz crystal producing a 9-MHz transfer rate, would be selected.

```
Channel mask for compliance test - ls bit is chnl 0
[0x0-0xffff]                              (0xffff) ->
```

Enter **0xffff** to select an HIA. Refer to Subtest 4999, *CONVEX Register Compliance Test*, in the "CONVEX PBUS I/O Systems Diagnostics Manual," for more information.

```
Default power margin for HIA chassis (+5 only)
[l,n,u]                                      (n) ->
```

Enter the power margin for the HIA chassis. The power margin may be changed to help debug hardware problems by forcing intermittent errors to hard errors.

- Enter **l** to select the lower power margin, 4.75 V.
- Enter **n** to select the nominal power margin, 5.00 V.
- Enter **u** to select the upper power margin, 5.25 V.

```
ATU scheme to test ('1' for C1, '2' for C2, 'b' for both)
[1,2,b]                                      (b) ->
```

Enter **1** if the test is to execute on a C1 or C120 machine. Enter **2** if the test is to execute on a C200 Series machine. Enter **b** for both ATU schemes to test on a machine.

> **NOTE**
>
> If **b** is entered, some subtests will take twice as long to execute.

```
Enter OK, or :NN to return to question NN [OK]
                                             (OK) ->
```

If **OK** or RETURN is entered, the "Example Test Parameter Menu" terminates and all inputs are

no longer changeable.

When all prompts have been answered, the screen displays a test parameter summary that echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure io4120–4, Sample Test Parameter Summary

```
                TEST PARAMETER SUMMARY

Hsp ccu slot number                          : 2
Hsp default clock rate                       : 0
Hia outclk default rate                      : 0
Hia busclk default rate                      : 0
Channel mask for compliance test - ls bit is chnl 0
                                             : 0xffff
Default power margin for HIA chassis (+5 only)
                                             : n
ATU scheme to test ('1' for C1, '2' for C2, 'b' for both)
                                             : b
Enter OK, or :NN to return to question NN : OK
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- Calls a routine to read Population Configuration Map (PCM) to determine where main memory is
- Allocates SPU windows for use in test
- Resets system through Scan Interface
- Turns on clocks for HSP
- Sets up software to be aware of hard and soft errors
- SPU local test variables are initialized
- Displays a "Test Parameter Summary"

After all the above events have occurred, the test code is started.

Class Descriptions

The *io4120* test has four classes of subtests as shown in the following table:

Table io4120–2, *io4120* Test Classes

CLASS	DESCRIPTION
1	68000 subsystem tests
2	HSP standalone tests
3	for use by CONVEX manufacturing only
4	HSP/HIA tests
5	HSP/HIA/FSE tests

Class 1 Subtests

Class 1 subtests verify that the HSP can correctly load a program from main memory. Class 1 subtests reside in the HSP EPROM and communicate with the SPU via the LED and the auxiliary test result registers on the HSP scan ring.

NOTE

The following are restrictions on the execution sequence of these subtests:

- Subtest 100 must be the first subtest in this class executed
- Subtests 101 and 102 may be executed in any order and may be executed in a loop until a failure occurs. If a failure occurs, Subtest 100 must be re-executed.
- After Subtest 103 is executed, Subtest 100 must be re-executed.

It is recommended that these tests be executed in numerical order.

The Class 1 subtests are listed in the following table:

Table io4120–3, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
100	HSP Reset	<:02
101	HSP Self-test	01:20
102	HSP Memory Initialization	<:02
103	HSP Boot	<:02

Subtest 100, HSP Reset

Subtest 100 resets the HSP via the scan ring. This causes the HSP to execute the initialization code in its EPROM. The initialization code saves the state of the HSP as found on reset and verifies that the HSP 68000 can calculate a checksum. When verified, the HSP calculates a checksum of the EPROM. If these tests pass, the HSP enters a loop and waits for an EPROM command to be placed on the LED register. If this test fails, the HSP informs the SPU by asserting a hard error (a double bus fault) which causes the 68000 to stop executing instructions.

Subtest 101, HSP Self-Test

Subtest 101 is the HSP self-test and consists of 10 steps that verify the ability of the HSP to load a program from main memory. The SPU commands the HSP to perform this test by placing a code in the HSP LED registers via the scan ring. When this code is detected, the HSP performs the steps listed below. If a failure is detected, the HSP returns the step number and other relevant data via the LED and auxiliary test result register.

Step 1: Verify Instructions Needed for Memory Test

Step 1 performs the following:

- Tests HSP 68000 registers
- Checks addressing modes
- Verifies jump and branch instructions
- The following operations are executed:
  - Integer arithmetic tests
  - Data movement operations
  - Shift and rotate instructions
  - Bit manipulation

Step 2: Initial Memory Operations Test

Step 2 determines the size of memory by writing to the first word in each bank until a bus error occurs. A walking '1' and '0' test is performed on the first word after the ROM and on the first word of the following banks. Then a uniqueness test and a true/complement pattern test is performed on the last 4 Kbytes of installed memory. Memory parity is checked by writing a word with inverted parity and then reading it to generate a parity error. The word is then rewritten with the correct parity.

Step 3: Verify Remaining 68000 Instructions

Step 3 uses the last 4 Kbytes of installed memory as a stack and checks the 68000 instructions not tested in Subtest 100 or in step 1 of this subtest. However, the *stop*, *trace*, and *reset* instructions are not checked. Step 3 also checks privilege violations and address errors.

Step 4: Test Remaining Memory

Step 4 is similar to step 2, but it checks memory from immediately after the ROM to the word preceding the last 4 Kbytes of installed memory. A parity test is not performed.

Step 5: Verify HSP Local Memory Protection

Step 5 performs a walking '1' and '0' test on the memory protection register at `0xff8000`. A uniqueness test and a true/complement pattern test is performed on all 256 registers. The test copies the HSP ROM into its memory, modifies the protection for installed memory to valid, read, write, and execute. Then the registers are cleared for uninstalled memory. Memory protection is turned on, and the valid, read, write, and execute bits are verified from the supervisor state and from the user state. At the end of the test, memory protection is disabled.

Step 6: Input Bus Test

Step 6 tests input bus integrity by pattern testing a longword in ATU memory. ATU memory is in two different address spaces in the HSP. The first address space checks the lower 32 bits of the input bus, and the second checks the upper 32 bits. The same 32 bit memory location is checked in both address spaces.

Step 7: PMAP Register Test

Step 7 tests the memory that stores the PMAP register data by performing column functionality, uniqueness, and bit functionality tests. Bad parity detection is then checked. Then a functionality test of the valid bit in the PMAP register is performed.

Step 8: Not Used

Step 8 is not used in the self-test in order to be able to distinguish a failure of a given self-test step from a HSP that has not started execution of its self-test. The value of 8 is used by the SPU to command the HSP to perform its self-test. As the HSP self-test executes, the value is incremented. By skipping step 8, the SPU can determine if the HSP started execution of its self-test.

Step 9: PBUS Header Generation

Step 9 checks the HSP PBUS header generation function by asserting the PBUS_TEST bit in the FDR register. Headers are generated for physical addresses of zero, all ones, walking zero, and walking one for both reads and writes in 8-bit and 16-bit access modes. When a header is generated, it is verified by inspection of the PBUS_HDR register. PBUS data is not transferred in during this test.

Step 10: PBUS Access Test

Step 10 performs a PBUS access test that reads, verifies, and echos a pattern placed in main memory by the SPU. This test verifies that the SPU and the HSP agree on the location of main memory and on the proper byte ordering in that memory. On C100 Series machines, the first access to the PBUS made by the HSP is to read the PCM. The PCM is used to locate the test pattern in main memory. On C200 Series machines, a register on the PBUS Interface Adapter (PIA) is read to locate the test pattern in main memory.

Subtest 102, HSP Memory Initialization

Subtest 102 initializes HSP memory after the local memory size is determined. The local memory is cleared from the word following the end of the EPROM to the end of installed memory. ATU memory and the device buffer memory is then initialized. The first PMAP register is pointed to the PCM and is searched for the first 2 Mbytes of physical memory. Once located, the map registers are initialized to point to the first 1 Mbyte of installed memory. The CCU slot number is used to index into a table in main memory. This table contains a 32-bit pattern initialized by the SPU. The HSP reads this pattern and returns it to main memory. The returned pattern is verified by the SPU. The pattern is the current time, in seconds, logically ANDed with a mask of `0xffffff00` and logically ORed with the CCU slot number.

Subtest 103, HSP Boot

> **NOTE**
>
> Before executing Subtest 103, Subtest 102 must have completed successfully. It is not possible to loop on this subtest.

Subtest 103 determines the size of local memory, and copies the EPROM to the last 16 Kbytes of installed local memory. A checksum is performed on local memory to verify it. The test sets memory protection for installed local memory to valid, read, write, and execute. The memory protection registers for uninstalled local memory are cleared. The interrupt status register is then cleared, and the HSP jumps to the local memory copy of the EPROM. Memory protection is enabled. The HSP slot number is used as an index into a table in main memory. The table is located in the first 1 Mbyte of installed main memory.

After the test begins, the HSP enters a loop while waiting for the SPU to place commands in main memory. The valid commands are listed in the following table:

Table io4120–4, Valid SPU Commands for Subtest 103

COMMAND	DESCRIPTION
load	Copies main memory to HSP memory, a byte at a time. As each byte is moved, *load* tallies it into a checksum. After main memory is moved, it checks for parity errors. If no errors, the checksum is placed in main memory; otherwise, negation of calculated checksum goes in main memory. At completion, *load* waits for more commands.
reset	Simulates a reset by loading the supervisor-stack pointer (ssp) from memory location 0 and the *pc* from memory location 4.
jump	Jumps to the address specified in main memory. The *ssp* is set to the top of installed local memory.

> **NOTE**
>
> Subtest 103 checks only the *load* command.

Class 2 Subtests

Class 2 subtests test the HSP without a device attached to the HSP. This class of subtests is loaded into the HSP local RAM from main memory. The following functions are tested:

- PBUS interrupt operations
- HSP address translation
- Address translation error detection
- Output bus integrity
- Error status register verification
- Line clock interrupt operation

The following table lists the Class 2 subtests:

Table io4120–5, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
210	PBUS Interrupt	00:36
220	PBUS Test-and-Set	<:02
230	ATU Memory Pattern	<:02
231	CSR Memory Pattern	<:02
232	Output Bus	<:02
233	Device Buffer Memory Pattern	<:02
240	ATU Local Translation—Physical Addresses	<:02
241	ATU Local Translation—Virtual Addresses	<:02
250	ATU Virtual Address Translation	<:02
251	ATU Memory Parity Error Detection	<:02
252	ATU *pte* Error Detection	<:02
270	Status Register Verification	<:02
280	Line Clock Interrupt	00:10

Subtest 210, PBUS Interrupt

Subtest 210 verifies the ability of the HSP to request and use the PBUS interrupt bus. It consists of three steps: an interrupt receive test, an interrupt transmit test, and an interrupt loopback test.

> **NOTE**
>
> The terms receive and transmit are from the perspective of the HSP.

Step 1: Receive Test

In the receive test, all 256 PBUS interrupts are sent by the SPU to the HSP, one at a time. After each interrupt is sent, the HSP verifies that only one interrupt was received

and that the interrupt was received by the proper group. The group in which each interrupt is received is determined by taking the modulo 4 residue of the interrupt number.

Step 2: Interrupt Transmit Test

In the interrupt transmit test, the HSP sends the SPU interrupt numbers 8, 9, 10, and 11, the four interrupts that the SPU is capable of receiving. The HSP verifies that the acknowledge for each interrupt is received and the SPU verifies the reception of the four interrupts.

Step 3: Interrupt Loopback Test

The interrupt loopback test causes all 256 interrupts to be sent and received by the HSP in each of the four possible groups. Like the receive test, as each interrupt is sent the HSP verifies that only one interrupt is received and that the acknowledge is also received.

Subtest 220, PBUS Test-and-Set

Subtest 220 verifies that all PMAP registers operate in test-and-set mode by placing each PMAP register in test-and-set mode in sequence. The PMAP register that logically follows the register under test is prepared for nontest-and-set operation and it verifies the operation.

A byte in the main memory command table is set to zero through the check window. It is read through the test window and the value returned is checked for a zero. The check window reads the byte in main memory and the value read is expected to be `0xff`. A second access through the test window verifies that the returned value is also `0xff`.

Subtest 230, ATU Memory Pattern

Subtest 230 performs column functionality, uniqueness, and bit functionality tests on the memory used by the Address Translation Unit (ATU) controller. It verifies that memory parity checking is operational by writing a byte with bad parity, reading it, and verifying that a parity interrupt occurs.

Since the PMAP registers and the ATU share a common memory, a uniqueness test over the two address spaces is also performed.

Subtest 231, CSR Memory Pattern

Subtest 231 tests the channel status memory by performing column functionality, uniqueness, and bit functionality tests. There is no parity on the Channel Status Register (CSR) memory.

Subtest 232, Output Bus

Subtest 232 checks the output bus by pattern testing two 32-bit words in the buffer memory used in device transfers. The first 32-bit location tests the bus in bit locations <31..0>, and the second checks the bus in bits <63..32>. Patterns of zero, all ones, alternating ones and zeros, walking ones, and walking zero are used in the subtest.

Subtest 233, Device Buffer Memory Pattern

Subtest 233 checks the device buffer memory for column functionality, uniqueness, and bit functionality. Parity is checked in the same way as in Subtest 230, ATU Memory Pattern.

Subtest 240, ATU Physical Address Mode Header

Subtest 240 checks the ability of the ATU controller to format PBUS headers while in physical address mode. The 68000 uses the File Description Register (FDR) register control bits to instruct the ATU to create PBUS headers.

ATU memory is initialized with the start address and byte count field such that the PBUS header is loaded with all zeros, all ones, a walking one, and a walking zero. As each header is generated, the ATU_OREG register is inspected for the correct header.

This subtest asserts the PBUS_TEST bit in the FDR register to inhibit the generated headers from being sent to the Multibus Control Unit (MCU) when the ATU is not functioning correctly.

Subtest 241, ATU Virtual Address Mode Header

Subtest 241 uses the FDR register to force the ATU to construct PBUS headers. The ATU memory is initialized so that the ATU constructs headers for data transfers, *pte* transfers, and *sdr* transfers in increasing levels of complexity. This is done by walking a one in the logical address that the ATU is translating. As each address is translated, the ATU_OREG register or the PBUS_HDR register, as appropriate, is checked for valid header contents.

This subtest asserts the PBUS_TEST bit in the FDR register to inhibit the generated headers from being sent to the MCU.

Subtest 250, ATU Virtual Address Translation

Subtest 250 checks the ATU logical address translation. The SPU fills a set of *sdr*s and *pte*s in main memory with pointers to nonexistent main memory. As the HSP walks a one through the logical address, it initializes only those locations in main memory and ATU memory that are required to complete the translation. As each translation occurs, the HSP verifies that the ATU only modified the needed locations in its memory. The *sdr*s and *pte*s in main memory are then restored to their initial state before the next logical address is checked.

Subtest 250 is executed for each ATU channel.

Subtest 251, ATU Memory Parity Error Detection

Subtest 251 tests the ATU parity error detection. It is tested by introducing a memory parity error into ATU register 6, the next address register, starting a translation, and verifying the error was logged in the CSR after the translation.

Subtest 252, ATU *pte* Error Detection

All *pte* entries used for HSP logical address translation must have bit <11> set to show that the selected *pte* is valid for I/O. Subtest 252 verifies that this bit is being checked by placing a *pte* level 2 in main memory without the bit set. A translation is started that reads the corrupted *pte*. The CSR register is checked for the global channel error flag set, as well as the I/O protection error.

The subtest is repeated with a corrupted *pte* level 1.

Subtest 270, Status Register Verification

Subtest 270 checks HSP error log recording functions by forcing various error conditions and verifying that they have been correctly reported. The subtest forces read, write, and execute errors on HSP local memory and verifies that they are reflected in the BERRLOG, ADDRHI, and ADDRLO registers.

PBUS read, write, and test and set errors are generated and the BERRLOG, PBERRLOG, ADRHI, and ADRLO registers are verified.

Finally, a DTACK timeout error is forced and the BERRLOG, ADRHI, and ADRLO registers are verified.

Subtest 280, Line Clock Interrupt

Subtest 280 enables the line clock interrupt on the HSP and waits for 600 line clock interrupts to occur. The SPU UNIX time of day is checked to ensure that the 600 interrupts took 10 seconds to occur.

Class 4 Subtests

Class 4 subtests verify the functionality of the HSP/HIA interface. These subtests are loaded into the HSP local memory from main memory and include tests for the following:

- Asynchronous and synchronous data transfers
- Address translation
- Clock selection
- Error detection and recovery

Table io4120–6, Class 4 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
4100	HIA Reset	00:22
4101	HIA Voltage	00:22
4110	Register Access—HSP clock 0	00:04
4111	Register Access—HSP clock 1	00:04
4112	Register Access—HSP clock 2	00:04
4113	Register Access—HSP clock 3	00:04
4120	Illegal Register Request	<:02
4130	Register Access Parity Error	<:02
4140	HIA Channel Interrupt	<:02
4180	Physical Address Read—HIA buffer 0	00:06
4181	Physical Address Read—HIA buffer 1	00:06
4182	Physical Address Write—HIA buffer 0	00:09
4183	Physical Address Write—HIA buffer 1	00:09
4184	Partial Longword Transfers	00:41
4190	Virtual Address Read Test—1 longword	00:12
4191	Virtual Address Read Test—2 longword	00:12
4192	Virtual Address Read Test—512 longword	00:12
4193	Virtual Address Read Test—513 longword	00:12
4194	Virtual Address Read Test—1000 longword	<:15
4195	Virtual Address Write Test—1 longword	00:26
4196	Virtual Address Write Test—2 longword	00:26
4197	Virtual Address Write Test—512 longword	00:25
4198	Virtual Address Write Test—513 longword	00:26
4199	Virtual Address Write Test—1000 longword	00:26
4200	HSP/HIA Clock Selection	04:16
4210	HSP Channel Functionality	00:11
4220	HSP ATU Parity Error Detection	<:02
4230	HSP I/O Access Bit Verification	<:02
4240	ATU PBUS Error Detection	00:06
4250	HSP Checkword Verification	<:02
4260	No Transfer Response	<:02
4270	Illegal Command Detection	<:02
4280	Data Parity Error Transfer	<:02
4990	HIA Internal Loopback—Buffer 0	<:02
4991	HIA Internal Loopback—Buffer 1	<:02
4992	HIA External Loopback—Buffer 0	<:02
4993	HIA External Loopback—Buffer 1	<:02
4994	HIA Local Slave Mode Transfer—Read	00:47
4995	HIA Local Slave Mode Transfer—Write	03:54
4999	CONVEX Register Compliance	<:02

Subtest 4100, HIA Reset

Subtest 4100 verifies that the HSP can reset the HIA. The HSP forces the HIA main controller to its idle condition. It then sets the DMAENA bit in the HIA CONTROL register and then asserts the reset signal to the HIA. The CONTROL register is then read and the subtest verifies that the

DMAENA bit has been reset.

Subtest 4101, HIA Voltage

Subtest 4101 measures and verifies the four voltages in the HIA chassis to ensure that they are within 5% of their nominal value. The nominal values used are +12V and -12V, and +5V and -5V.

Subtests 4110–4113, Register Access

Subtests 4110 through 4113 test the HSP asynchronous data transfer function (device register access) by pattern testing the following:

- HIA buffer memories in both 8-bit and 16-bit modes
- HIA parity memory in 8-bit mode
- The Direct Memory Access (DMA) register file in 16-bit mode
- The GLOMSK register in 16-bit mode

Uniqueness, bit, and column functionality tests are performed on each of the above. The interface clock is changed from 0 through 3 in Subtests 4110 to 4113 respectively.

Subtest 4120, Illegal Register Request

The HSP makes illegal requests to the HIA and expects the HIA to return an illegal register response code. Subtest 4120 verifies that the error is correctly logged in the HSP BERRLOG and ADDRHI/LO registers, and also in the HIA REGERR register. The following accesses are made to force the errors:

- 16-bit access to the HIA parity memory
- 8-bit access to the DMA register file
- 8-bit access to the HIA CONTROL register
- 8-bit and 16-bit accesses to a nonexistent register in the HIA address space

Subtest 4130, Register Access Parity Error

Subtest 4130 verifies that parity generation and detection is working for register accesses. The HSP makes a register access request with bad parity in the opcode, address, and data fields. For each request, the HSP verifies that the HIA sends a command parity error response and that the register request ends in a bus error.

The HSP then corrupts the parity on a longword in the HIA buffer memory. Then a register access is made to the corrupted location and the subtest expects the register access to result in a bus error and the HIA to have sent a fatal error response to the HSP.

Subtest 4140, HIA Channel Interrupt

The HSP resets the HIA by asserting the reset line on the HSP interface. The HSP then reads the HIA GLOINT register and clears the HIA FIR to clear any pending interrupts. The HSP then disables device interrupts in the HSP IER.

The subtest then uses the HIA FIR register to force a channel interrupt for each channel. For channel zero, the subtest verifies that the interrupt does not occur until the interrupt enable bits in the HIA CONTROL register and the HSP IER register are set. For all channels, the subtest verifies that the interrupt does not occur until the channel interrupt is enabled in the HIA IER.

Subtests 4180–4183, Synchronous Data Transfers with Physical Addresses

These subtests exercise the HSP synchronous data transfer functions without address translation. The amount of data and the addresses used in the subtests varies. These combinations test the HSP end of logical page detection and data buffer valid flush operations. The subtests are divided into reads and writes. A data equals address pattern is used in all subtests. After each transfer, the destination area is checked to verify that all the data was transferred and that no additional data was written. All data lengths and addresses are longword aligned. Each subtest tests the data transfers with a sliding one and zero in the least significant 12 bits of the address.

Subtest 4184, Partial Longword Transfers

Correct handling of partial longword transfers is verified by programming the HIA to transfer various transfers each with a different starting address and byte count. The addresses range from logical address 0 to logical address 16 and the byte count varies from 1 to 16. This causes all combinations of leading partial, block transfer, and trailing partial to be tested.

Subtests 4190–4199, Virtual Address Read and Write

These subtests exercise the HSP synchronous data transfer logical address translation operation. They vary in the amount of data they transfer and in the direction of the transfer. All data is longword aligned. The subtest virtual addresses are generated by sliding a one from bit <3> through bit <31>. This causes the address translation logic to be checked in an incremental fashion. For all transfers, only the required ATU memory is initialized with valid data. The remaining portions are initialized with pointers to nonexistent main memory. A data equals address pattern is used for all transfers. The destination is initialized to the negation of these patterns for each transfer attempted. After each transfer, ATU memory registers 0, 1, 3, 4, 5, and 11 are checked for the expected values. The destination area is checked for valid data.

Subtest 4200, HSP/HIA Clock Selection

Subtest 4200 tests the various data rates available for synchronous data transfers. For each possible clock combination, a 32-Kbyte transfer is initiated. After the transfer, the destination is read to verify data integrity. Reads and writes are both tested.

Subtest 4210, HSP Channel Functionality

Subtest 4210 verifies that all HSP channels are functional by starting a 32 Kbyte transfer on each one. After the transfer, the destination is read to verify data integrity. Reads and writes are both tested.

Subtest 4220, HSP ATU Parity Error Detection

Subtest 4220 verifies ATU parity error detection synchronous data transfers. The 68000 initializes ATU memory in a normal fashion except that register 11 is initialized with inverted parity. The HIA is programmed to perform one longword read from main memory. After the transfer, the subtest verifies that the CSR logs the error as a memory parity error during a Segment Descriptor Register (SDR) read. Additionally, the CSR is checked to ensure that the NEW_SDRS bit is set, the channel enable is reset, and that the global error bit is set.

Subtest 4230, HSP I/O Access Bit Verification

Subtest 4230 verifies that the I/O access bit of *pte* levels 1 and 2 is processed correctly. For each *pte* level, a set of *pte*s is initialized in main memory with one valid entry and all others invalid. A 1-longword transfer is started from a valid logical address. The subtest verifies transfer completion without error. For PBUS reads, this verifies that a prefetch from a protected area does not produce an error response by the HSP if the data was not sent to the HIA. A second 2-longword transfer is then started. This causes the HSP to try to send data from a page without I/O access enabled. The subtest expects that the CSR will reflect an I/O protection error, that the NEW_SDRS bit is set along with the global error flag, that the *pte* level where the error occurred is properly encoded in the CSR, that the direction of the transfer is also properly saved in the CSR, and that the channel enable bit is reset. The subtest verifies both reads and writes.

Subtest 4240, ATU PBUS Error Detection

Subtest 4240 verifies that the HSP can recover from PBUS errors received during various stages of processing. Initially, a pair of *pte*s level 2 are initialized in main memory. The first contains a pointer to a valid location in main memory, the second contains a pointer to nonexistent memory. A one longword transfer is started such that the data used comes from the valid page and the prefetch (on reads) comes from the nonexistent page. Then the subtest verifies that the transfer completes without error. For reads, the subtest verifies that the NEW_SDRS bit is set in the CSR.

The operation is restarted with a longword count that causes the data from the second page to be used. The CSR is checked to verify that it has the PBUS_BUS_ERROR bit set, that the CSR shows the error as having occurred during a data access, and that the CSR has the enable bit turned off and the NEW_SDRS bit on.

The above procedure is repeated moving the bad memory pointer from a *pte*2 to a *pte*1, *sdr*, and finally to the pointers to the *sdr*s changing the expected error condition appropriately. Both reads and writes are verified.

Subtest 4250, HSP Checkword Verification

Subtest 4250 verifies the proper operation of the HSP checkword by causing the HIA to do a write to main memory of a single longword with an incorrect checkword. The checkword is corrupted one bit at a time for each of the 64 bits of a longword. After each transfer, the ATU CSR is checked to verify that the checkword error bit is set.

Subtest 4260, No Transfer Response

Subtest 4260 verifies the functionality of the channel enable bit by having the HIA start a transfer on a channel without the enable bit set. It also verifies that the HSP sent a no transfer response code.

Subtest 4270, Illegal Command Detection

Subtest 4270 causes the HIA to send a partial write request for an illegal address/byte count combination. The subtest verifies that the HSP sends an invalid command response to the HIA. The CSR is checked to make sure that an error is not logged in the CSR.

Subtest 4280, Data Parity Error Transfer

Subtest 4280 verifies that the HSP can detect data parity errors during synchronous transfers. The subtest programs the HIA to send data with inverted parity. Each of the 8 bytes in a longword is tested in succession. After each transfer, the ATU CSR is checked to ensure that the parity error was logged, the HSP is expected to have sent the HIA a block checksum parity error response code, and the IBPAR register on the HSP is read to verify that the correct byte in error was logged.

Subtest 4990, 4991, HIA Internal Loopback

These subtests verify the integrity of the data alignment bus internal to the HIA. One of the two data buffers in the HIA is initialized with a pattern of walking '1's and walking '0's. The HIA is programmed to transfer the initialized buffer into the other HIA buffer. The destination buffer is then checked for data integrity. Subtest 4990 copies HIA buffer 0 to buffer 1. Subtest 4991 copies buffer 1 to buffer 0.

Subtest 4992, 4993, HIA External Loopback

These subtests verify data bus integrity on the user interface. One of the two HIA data buffers is initialized to a pattern of walking '1's and walking '0's. The initialized buffer is then transferred to the other buffer and the destination is checked for data integrity. The test is repeated for all four data port sizes. For data port sizes less than 64 bits, the unused portions of the data bus are initialized to the contents of the used portion, thus, the data pattern is modified in the loopback process. Subtest 4992 copies HIA buffer 0 to buffer 1. Subtest 4993 copies buffer 1 to buffer 0.

Subtest 4994, 4995, HIA Local Slave Mode Transfers

These subtests verify that the HIA can transfer data in a pseudo slave mode. The subtest tests all data port sizes for logical addresses from 0 to 7, for byte counts of 1 to 16, 4072 to 4089, and 8000 to 8015. After each transfer, the subtest verifies that no errors were logged and that the data was transferred correctly. Subtest 4994 tests transfers to the HIA, and Subtest 4995 tests transfers to main memory.

Subtest 4999, CONVEX Register Compliance

Subtest 4999 verifies that the device attached to the HSP complies with the HIA standards. The register at `0xc00000` is read and its contents is verified to be one of, `0x0080`, `0x0010`, `0x0020`, `0x0020`, or `0x0030`. All valid values will cause a device interrupt test to be performed in the same fashion as Subtest 4140, Channel Interrupt Test, except that the user may specify on which channels the test is to be performed by answering the correct prompt when *io4120* is invoked. If the value read from the id register at `0xc00000` is `0x0020`, `0x0040`, or `0x0080`, a read of `0xc00086` is made to verify the presence of the GLOINT register. If the value read from the id register is `0x0030`, `0x0040`, or `0x0080`, a read of a portion of the DMA channel memory is made for all channels specified by the user. Each channel will have a read made for registers at offsets of 0 through `0xe`.

Class 5 Subtests

Class 5 tests verify the functionality of the user interface on the HIA, including:

- Register access to user device address space
- User device register error detection and correction
- User interface interrupts
- Data transfers to and from the user device in all data port sizes and data alignment addresses
- Data transfers in all four data transfer modes
- User interface handshake tests
- Data modulation tests
- User interface error detection and recovery
- Correct operation at all possible clock rates

The Class 5 subtests are listed in the following tables:

Table io4120–7, Class 5 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
5000	User Interface Reset	<:02
5010	FSE RAM	<:02
5020	User Register Error	<:02
5030	User Interrupt	<:02
5180	HIA/FSE Small Read–64-bit datum	<:02
5181	HIA/FSE Small Read–32-bit datum	00:04
5182	HIA/FSE Small Read–16-bit datum	00:09
5183	HIA/FSE Small Read–8-bit datum	00:18
5184	HIA/FSE Large Read–64-bit datum	00:03
5185	HIA/FSE Large Read–32-bit datum	00:06
5186	HIA/FSE Large Read–16-bit datum	00:14
5187	HIA/FSE Large Read–8-bit datum	00:39
5190	HIA/FSE Small Write–64-bit datum	<:02
5191	HIA/FSE Small Write–32-bit datum	00:05
5192	HIA/FSE Small Write–16-bit datum	00:11
5193	HIA/FSE Small Write–8-bit datum	00:24
5194	HIA/FSE Large Write–64-bit datum	00:03
5195	HIA/FSE Large Write–32-bit datum	00:07
5196	HIA/FSE Large Write–16-bit datum	00:17
5197	HIA/FSE Large Write–8-bit datum	00:42
5200	32k Slave Mode Read–64-bit datum	00:05
5201	32k Slave Mode Read–32-bit datum	00:03
5202	32k Slave Mode Read–16-bit datum	00:03
5203	32k Slave Mode Read–8-bit datum	00:03
5204	32k Slave Mode Write–64-bit datum	00:04
5205	32k Slave Mode Write–32-bit datum	00:04
5206	32k Slave Mode Write–16-bit datum	00:04
5207	32k Slave Mode Write–8-bit datum	00:03
5300	32k Chain Mode Read–64-bit datum	00:04
5301	32k Chain Mode Read–32-bit datum	00:04
5302	32k Chain Mode Read–16-bit datum	00:04
5303	32k Chain Mode Read–8-bit datum	00:03
5304	32k Chain Mode Write–64-bit datum	00:05
5305	32k Chain Mode Write–32-bit datum	00:04
5306	32k Chain Mode Write–16-bit datum	00:03
5307	32k Chain Mode Write–8-bit datum	00:03
5400	32k Normal Mode Transfer–64-bit datum	00:08
5401	32k Normal Mode Transfer–32-bit datum	00:06
5402	32k Normal Mode Transfer–16-bit datum	00:06
5403	32k Normal Mode Transfer–8-bit datum	00:06
5500	32k Extended Mode Transfer–64-bit datum	00:07
5501	32k Extended Mode Transfer–32-bit datum	00:06
5502	32k Extended Mode Transfer–16-bit datum	00:06
5503	32k Extended Mode Transfer–8-bit datum	00:06

Table io4120–7, Class 5 Subtests (continued)

SUBTEST	DESCRIPTION	TIME (hr:min:sec)
5600	Kill Channel	00:04
5610	Data Modulation	00:55
5620	DMA Enable Bit	00:01
5640	Data Parity Detection	00:05
5650	Transfer Error from HSP	00:20
5660	User Read Parity Error Signal	<:02
5670	Clock Selection	4:03:06

Subtest 5000, User Interface Reset

Subtest 5000 verifies that the HSP can reset the HIA. The HSP forces the HIA main controller to its idle condition. It then sets the DMAENA bit in the HIA CONTROL register and then asserts the reset signal to the HIA. The CONTROL register is then read and the subtest verifies that the DMAENA bit has been reset.

Subtest 5000 then reads the FSE errstat register and verifies that the power-up bit is cleared. The subtest then resets the user device by clearing the HIA CONTROL register, and setting the HIA CONTROL user run bit. The FSE errstat register is then reread and the subtest expects the power up bit to be set.

Subtest 5010, FSE RAM

Subtest 5010 consists of bit, column, and uniqueness tests for the FSE data buffer RAM and the FSE command queue. The data buffer RAM tests are performed twice, once using 16-bit accesses and once using 8-bit accesses. The command queue ram is only tested with 16-bit accesses.

Subtest 5020, User Register Error

The NORESPON, BADACK, and BADERR registers on the FSE are read to force a register access error. This subtest verifies that each access results in a bus error.

The subtest then reads register addresses starting with `c20001` and slides the one bit until the address is `c30000`. For each access, the subtest expects a bus error. After each access, the FSE LASTADRH and LASTADRL registers are read and verification is made that the address was latched correctly.

The parity on a 16-bit word in the FSE data buffer is then corrupted and the subtest verifies that reading that location results in a bus error. Each of the two parity bits in the word is checked individually.

Subtest 5030, User Interrupt

Subtest 5030 uses the FSE interrupt register to force an interrupt condition to the HIA. When first asserted, user interrupts are masked in the HIA GLOMSK register. The subtest verifies that no interrupt is sent to the HSP and that the interrupt is logged in the HIA GLOINT register. User interrupts are then unmasked, and the subtest verifies that the HSP receives the interrupt and that it can clear the interrupt by writing to the FSE interrupt register.

Subtest 5180–5187, 5190–5197, HIA/FSE Local Transfers

This series of subtests verify that the HIA and FSE can transfer data across the user interface. No synchronous data is transferred to or from the HSP. The subtests vary in the number of bytes transferred, the direction of the transfer, and the data port size used. The subtests listed as small transfers in the Class 5 Subtests table use byte counts of 1 to 16, inclusive. Subtests listed as large use byte counts of 4,080 to 4,096. For each iteration of the byte count, the subtest varies the logical address used from zero to seven, inclusive, in order to test all possible data alignments.

The HSP initializes the source and destination memory areas by register access. The HIA is then programmed to perform the transfer and the transfer is started. After the transfer, the HSP checks the HSP and HIA error registers and then reads the destination area to verify the data was transferred correctly.

Subtest 5200–5207, Slave Mode Transfers

This series of subtests verify that the HSP/HIA/FSE can transfer data in slave mode. Each subtest transfers 32-Kbytes. The subtests vary in the direction of the transfer and in the data port size used. Each subtest varies the logical address used from zero to seven, inclusive, in order to test all possible data alignments.

The HSP initializes the source and destination memory areas by register access. The HSP/HIA/FSE is then programmed to perform the transfer. After the transfer, the HSP checks the HSP/HIA/FSE error registers and then reads the destination area to verify the data was transferred correctly. All transfers take place on channel zero.

Subtest 5300–5307, Chain Mode Transfers

This series of subtests verify that the HSP/HIA/FSE can transfer data in chain mode. Each subtest transfers 32k bytes. The subtests vary in the direction of the transfer and in the data port size used. Each subtest varies the logical address used from zero to seven, inclusive, in order to test all possible data alignments.

The HSP initializes the source and destination memory areas by register access. The HSP/HIA/FSE is then programmed to perform the transfer. Each of the 16 channels is programmed to transfer one-sixteenth of the data. The last channel in the chain is disabled in the HIA. The transfer is then started on the first 15 channels. After the transfer, the subtest verifies that the first 15 channels finished without any error. The enable bit on the last channel is then set, and the subtest expects the last channel to transfer its data. After the transfer, the HSP checks for errors, and then reads the destination area to verify the data was transferred correctly.

Subtest 5400–5403, Normal Mode Transfers

This series of subtests verify that the HSP/HIA/FSE can transfer data in normal mode. Each subtest transfers 32-Kbytes. The subtests vary in the the data port size used. All subtests in this range are read/write subtests. Each subtest varies the logical address used from zero to seven, inclusive, in order to test all possible data alignments.

These subtests program the HSP/HIA/FSE to transfer data from main memory to the FSE, and then from the FSE back to a second location in main memory. The channels are programmed to transfer the data in such a manner that a read is followed by a write, then another read, and then another write. This verifies that all read/write combinations are functional.

After the transfer, the subtest verifies that the data in the FSE is correct and then it verifies that the second copy in main memory is correct.

Subtest 5500–5503, Extended Mode Transfers

This series of subtests verify that the HSP/HIA/FSE can transfer data in extended mode. Each subtest transfers 32-Kbytes. The subtests vary in the data port size used. All subtests in this range are read/write subtests. Each subtest varies the logical address used from zero to seven, inclusive, in order to test all possible data alignments.

These subtests program the HSP/HIA/FSE to transfer data from main memory to the FSE, and then from the FSE back to a second location in main memory. The channels are programmed to transfer the data in such a a manner that a read is followed by a write, then another read, and then another write. This verifies that all read/write combinations are functional.

After the transfer, the subtest verifies that the data in the FSE is correct and then it verifies that the second copy in main memory is correct.

Subtest 5600, Kill Channel

Subtest 5600 verifies that the HIA can process kill channel signals correctly. Kill channel processing is tested by programming transfers in all four transfer modes, and then having the FSE assert kill channel. Each transfer mode is tested for both reads and writes. After the signal has been asserted, the subtest verifies that the appropriate fields in the HIA and FSE were updated correctly. Transfers in slave and chain mode are expected to terminate the transfer on all subsequent channels after the signal is asserted. Transfers in normal and extended mode are expected to terminate only the channel on which the signal is received. Subsequent channels are expected to complete without error.

Subtest 5610, Data Modulation

Subtest 5610 verifies that the HIA can process the read/write signals from FSE. The correct handling of the read/write handshake lines on the user interface is tested by programming the FSE to transfer data while modulating the handshake lines at varying intervals. After the transfer, the subtest verifies that the data was transferred correctly.

Subtest 5620, DMA Enable Bit

Subtest 5620 verifies that turning off the DMA enable bit on an active channel will shut down a transfer in a graceful manner. The FSE is programmed to perform a transfer and then have it hold off sending or receiving data for many clock cycles to give the HSP a chance to turn off the DMA enable bit. The subtest then verifies that the data transferred before the hold command is correct. Both reads and writes are tested in normal and extended transfer modes.

Subtest 5640, Data Parity Detection

Subtest 5640 verifies that HIA data parity checkers on the user interface are operational. The FSE is programmed to send the HIA data with bad parity in it. The test is made in each of the four transfer modes. For slave and chain modes, the subtest verifies that the transfer stops after the error is encountered and that the HIA resets the DMA enable bit in its control register. For normal and extended mode, the subtest verifies that only the channel where the error was made is disabled and the rest of the transfer finishes normally. For all transfer modes, the register file is examined to verify that the error is properly logged.

Subtest 5650, Transfer Error from HSP

Subtest 5650 verifies that the HIA can process transfer error responses from the HSP. Two transfers are programmed which result in the HSP sending a *no transfer* response and a *fatal error* response. These two error responses are generated for reads and writes in each of the four transfer modes for both reads and writes. Errors in slave and chain modes are expected to terminate the transfer. Errors in normal and extended mode are expected to terminate the transfer on the channel receiving the error and continue with the remaining channels.

Subtest 5660, User Read Parity Error Signal

Subtest 5660 verifies that the HIA can process the user read parity error signal correctly. A read transfer is programmed in which the FSE asserts the ReadParErr signal. The subtest verifies that the HIA logs the error correctly. Errors in slave and chain modes are expected to terminate the transfer. Errors in normal and extended mode are expected to terminate the transfer on the channel receiving the error and continue with the remaining channels.

Subtest 5670, Clock Selection

Subtest 5670 performs Subtests 5200 through 5507 varying the HSP clock, HIA outclk, and HIA busclk over all possible clock combinations. It does not change the system backplane clock. Two passes through all the possible clock rates are made. The first pass forces the HIA to throttle the data, and the second pass does not.

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io5000

VMEbus I/O Processor Test

Overview

The *io5000* test verifies the functionality of a specified VIOP. The test verifies the following on the VIOP(s) specified:

- 68020 on the VIOP can correctly execute instructions
- VIOP local memory is functional
- Memory protection and mapping registers are operational
- Cache memory can be written to and read from, and the associated cache control bits are functional
- Two VMEbus cable interfaces operate in loopback mode
- VIOP can boot a program from memory
- Voltages on all installed VMEbus chassis are within tolerance

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test.

Table io5000–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
VIOP	VIOP
VBCU	VBCU
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Test Invocation

The *io5000* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *io5000* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure io5000–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test io5000 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test io5000** executes all *io5000* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure io5000–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test io5000 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure io5000–3, Test Parameter Menu

```
                ENTER TEST PARAMETERS

[]      Encloses allowed input ranges or values
()      Encloses the default value
^       Returns to the previous prompt
:nn     Returns to the prompt # nn
:       Returns to the first unsatisfied prompt
:?      Reviews previous entries

 1: Enter VIOP numbers [0123][1]                    (1) ->
 2: Enter value for Disable_68k_cache flag [0,1]
                                                    (0) ->
 3: Enter OK, or :NN to return to question NN [OK]
                                                   (OK) ->
```

[1] The possible selections for this prompt can vary depending on the machine architecture.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

A description of the meaning of each prompt follows:

```
Enter VIOP numbers [0123]                    (1) ->
```

This prompt allows selection of the VIOP(s) to be scanned. For more than one VIOP, enter the numbers contiguously, i.e., 012. After entering the VIOP number(s), each VIOP entered is scanned to see if it exists. Any invalid number causes the test to reprompt for valid VIOP(s). The test executes only when all entries are valid.

```
Enter value for Disable_68k_cache flag [0,1]
                                             (0) ->
```

This prompt allows modification of the setup of the VIOP scan ring bit that can force the 68020 to run with its internal instruction cache disabled. Disabling the 68020 cache forces a memory reference for each instruction fetch.

```
Enter OK, or :NN to return to question NN [OK]
                                            (OK) ->
```

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The SPU verifies that the selected VIOPs are installed by scanning patterns into the VIOP LED register
- Verifies that the system has been reset since power-up

After all the above events have occurred, the test code is started.

Class Descriptions

The *io5000* contains the following six classes of subtests:

Table io5000–2, *io5000* Test Classes

CLASS	DESCRIPTION
1	68020 subsystem tests
2	VIOP miscellaneous tests
3	Cache functionality tests
4	Interrupt tests
5	VBCU interface tests
6	VMEbus voltage tests

NOTE

The first time one of the subtests in the 200 through 601 range is executed, the VIOP(s) under test must be loaded with the test program, which adds about 10 seconds to the test times.

Class 1 Subtests

Class 1 subtests verify that the VIOP can correctly load a program from main memory. Class 1 tests reside in the VIOP's EPROM and communicate with the SPU via the LED and the auxiliary test result registers on the VIOP scan ring.

NOTE

There are restrictions on the execution sequence of these subtests:

- Subtest 100 must be the first subtest executed in this class.
- Subtests 101 and 102 may be executed in any order and may be executed in a loop until a failure occurs. If a failure occurs, Subtest 100 must be re-executed.
- After Subtest 103 is executed, Subtest 100 must be re-executed.

It is recommended that these tests be executed in sequential order.

Table io5000–3, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (minsec)
100	VIOP Reset	:02
101	VIOP Self-test	:31
102	VIOP Initialization Command	:02
103	VIOP Boot Command	:02

Subtest 100, VIOP Reset

Subtest 100 resets the VIOP via the scan ring. This causes the VIOP to execute the initialization code in its EPROM. The initialization code saves the state of the VIOP as found on reset and verifies that the VIOP's 68020 can calculate a checksum. When verified, the VIOP calculates a checksum of the EPROM. If these tests pass, the VIOP enters a loop and waits for an EPROM command to be placed on the LED register. If this test fails, the VIOP informs the SPU by asserting a hard error.

Subtest 101, VIOP Self-test

Subtest 101 is the VIOP's EPROM based self-test. It consists of 11 steps that verify the VIOP's ability to load a program from main memory. The SPU commands the VIOP to do this test by placing a code in the VIOP's LED registers via the scan ring. When this code is detected, the VIOP executes the steps listed below. If a failure is detected, the VIOP returns the step number and other relevant data via the LED register and auxiliary test result register in the scan ring.

Step 1: Pattern Test the Auxiliary Test Results Register

Step 1 verifies that the Auxiliary Test Results Register (AUXTRR) is usable for reporting failure information back to the SPU in the event of a failure of one of the later steps.

Step 2: Verify Instructions Needed for Memory Test

Step 2 performs the following:

- Test VIOP 68020 registers
- Check addressing modes
- Verify jump and branch instructions
- The following operations are executed:
  - Integer arithmetic tests
  - Data movement operations
  - Shift and rotate instructions
  - Bit manipulation

Step 3: Initial Memory Operations Test

Step 3 determines the size of memory by writing to the first word in each bank until a bus error occurs. It performs a walking '1's and '0's test on the first word after the EPROM, and on the first word of the following banks. Then, on the last 4 Kbytes of installed memory, it does a uniqueness test and a true/complement pattern test. Memory parity is checked by writing a word with inverted parity and then reading it to generate a parity error. The word is then rewritten with the correct parity.

Step 4: Verify Remaining 68020 Instructions

Step 4 uses the last 4 Kbytes of installed memory as a stack, and checks the 68020 instructions not tested in Subtest 100, VIOP Reset Test or in step 2 of this subtest. The *stop*, *trace*, and *reset* instructions are not checked. It also checks privilege violations and address errors.

Step 5: Test Remaining Memory

Step 5 is similar to step 3, but it checks memory from immediately after the EPROM to the word preceding the last 4 Kbytes of installed memory. No parity testing is done.

Step 6: Verify VIOP Local Memory Mapper

Step 6 starts by doing a walking '1's and '0's test on the memory protection register at `0xff8000`. For all 256 registers, it does a uniqueness test and a true/complement pattern test. The test copies the VIOP's EPROM to its local RAM, modifies the protection for installed memory to valid, read, write, and execute. It clears the registers for uninstalled memory. Memory protection is turned on, and the valid, read, write, and execute bits are verified from the supervisor state and the user state. At the end of the test, memory protection is disabled.

Step 7: PMAP Register Test

The RAMs that store the PMAP register data are checked by performing column functionality, uniqueness, and bit functionality tests. Bad parity detection is then checked. This is followed by a functionality test of the valid bit in the PMAP register.

Step 8: Not Used

Step 8 is not used in the self-test in order to be able to distinguish a failure of a given step with a VIOP that never started executing. The value of 8 is used by the SPU to command the VIOP to perform its self-test. As the VIOP progresses in its test, the value is incremented. By skipping step 8, the SPU can determine if the VIOP started execution of the self test.

Step 9: VIOP Cache Test

Step 9 clears the cache after disabling cache parity checking and clearing the longword/byte dirty flags and the tag flag registers. Then it reclears the tag flag registers and enables cache parity checking. Any pending cache or PBUS interrupts are cleared, and cache interrupts are enabled. The local memory copy of the EPROM is mapped in, and a checksum is performed on it. Next, the test sets the map registers to point to the last Mbyte of the PBUS. A unique pattern is written to the first 64 shortwords in each main memory 4 Kbyte window. As each word is written, the dirty bits are checked to see that they are updated appropriately. The test then clears the longword/byte dirty flags and marks all tag registers as loaded. Finally, the pattern written to each cache location is verified.

Step 10: VME Cable Interface Loopback Test

Step 10 resets the VMEbus cable drivers and places them in loopback mode. A local memory copy of the EPROM is mapped in through each cable interface and a checksum test is performed. Then the pattern left by the cache test is checked through each of the VIOP cache windows.

Step 11: PBUS Access Test

Step 11 performs the PBUS access test which reads, verifies, and echos a pattern placed in main memory by the SPU. This test verifies that the SPU and the VIOP agree on the

location of main memory and of the proper byte ordering in that memory. The first access to the PBUS made by the VIOP is to read the Population Configuration Map (PCM). This is needed to locate the test pattern in main memory.

Subtest 102, VIOP Initialization Command

Subtest 102 determines the size of the installed local memory and then clears local memory from the word following the EPROM to the end. The test then disables cache parity checking. Subtest 102 performs the following for each of the map registers:

- Clears the dirty 'a' and 'b' bits
- Clears the corresponding 128 cache bytes
- Clears the dirty 'a' and 'b' bits again

Next, for C100 Series machines, the test enables cache parity checking, and points the first map register to the Population Configuration Map (PCM) on the MCU. The PCM is searched to locate the first 2 Mbytes of main memory. Once located, the map registers are initialized to point to the first half of this 2-Mbyte block. For C200 Series machines, the test reads the Memory Base Pointer (MBP) to determine the address of the first block of memory.

The motherboard slot number is used to index into a table in main memory. This table contains a pattern, previously initialized by the SPU, that is to be echoed by the VIOP. The pattern is the current time, in seconds, logically 'anded' with a mask of `0xffffff00`. When the VIOP echoes this pattern, the subtest ends.

Subtest 103, VIOP Boot Command

> **NOTE**
>
> Subtest 102 must have completed successfully before executing Subtest 103. It is not possible to loop on this subtest.

Initially, Subtest 103 determines the size of local memory and copies the EPROM to the last 32 Kbytes of installed local memory. A checksum is performed on local memory to verify it. The test sets memory protection for installed local memory to valid, read, write, and execute. The memory protection registers for uninstalled local memory are cleared. The interrupt status register is then cleared, and the VIOP jumps to the local memory copy of the EPROM. Memory protection is enabled. The VIOP slot number is used as an index into a table in main memory. The table is located in the first Mbyte of installed main memory.

After the test begins, the VIOP enters a loop waiting for the SPU to place commands in main memory by the SPU. The valid commands are listed in the following table:

Table io5000–4, Valid SPU Commands for Subtest 103

COMMAND	DESCRIPTION
load	Copies main memory to VIOP memory, a byte at a time. As each byte is moved, *load* tallies it into a checksum. After main memory is moved, it checks for parity errors. If no errors, the checksum is placed in main memory; otherwise, negation of calculated checksum goes in main memory. At completion, *load* waits for more commands
reset	Simulates a reset by loading the supervisor-stack pointer from memory location 0 and the *pc* from memory location 4.
jump	Jumps to the address specified in main memory. The *ssp* is set to the top of installed local memory.

NOTE

This subtest checks only the *load* command.

Class 2 Subtests

Class 2 subtests verify various parts of the VIOP that do not logically fall under any of the other classes. These subtests verify the next level of functionality past the EPROM based Class 1 subtests.

Table io5000–5, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	PBUS Communication	:16
220	PBUS Test-and-set	:02
221[1]	PBUS Test-and-clear	:02
230	Line Clock Interrupt	:10
250	VIOP Microprocessor Clock Margin	:18
251	VIOP Cache Buffer Tag	:52
261	Parity Checker	:01

[1] This subtest is only available on C200 Series machines.

Subtest 200, PBUS Communication

After the VIOP has been booted, Subtest 200 tests the ability of the SPU to communicate with the program running on the VIOP via main memory by sending 1,000 no-op commands to the VIOP. The SPU puts a command number in the communication structure in main memory and waits for the VIOP to write into the structure indicating completion of the command. In this case the VIOP interprets the command as a no-op and immediately signals that the command has been completed.

Subtest 220, PBUS Test-and-set

Subtest 220 verifies that all PMAP registers operate in test-and-set mode by placing each PMAP register in test-and-set mode in sequence. The PMAP register that logically follows the register under test is prepared for nontest-and-set operation and it verifies the operation.

A byte in the main memory command table is set to zero through the check window. It is read through the test window and the value returned is checked for a zero. The check window reads the byte in main memory and the value read is expected to be `0xff`. A second access through the test window verifies that the returned value is also `0xff`.

Subtest 221, PBUS Test-and-clear

> **NOTE**
>
> This test is only available for C200 Series machines and will not execute on a C1 or C120 machine.

Subtest 221 verifies that all PMAP registers operate in test-and-clear mode, by placing each PMAP register in test-and-clear mode in sequence. The PMAP register that logically follows the register under test is prepared for nontest-and-clear operation and is used to verify the operation.

A byte in the main memory command table is set to one through the check window. It is read through the test window and the value returned is checked for a one. The check window reads the byte in main memory and the value read is expected to be zero. A second access through the test window verifies that the returned value is also zero. The operation is repeated for all windows.

Subtest 230, Line Clock Interrupt

Subtest 230 enables the line clock interrupt on the VIOP and waits for 600 line clock interrupts to occur. The SPU UNIX time of day is checked to ensure that the 600 interrupts took 10 seconds to occur.

Subtest 250, VIOP Microprocessor Clock Margin

Subtest 250 tests the ability of the SPU to select the clock frequency for the VIOP microprocessor. The VIOP has two clock frequencies that can be selected to run the VIOP 68020 microprocessor.

The frequencies are generated by two separate clock oscillators. The nominal clock frequency is 20 MHz, and the alternate, or margin, clock frequency is usually 22 MHz. The alternate clock frequency is derived from a socketed oscillator which is divided by two to produce the alternate clock frequency. The socketed oscillator may be replaced with any value between 25 MHz and 44 MHz.

The test first sets all selected VIOPs to run from its standard or nominal clock frequency. The VIOPs are rebooted because selecting the clock frequency requires resetting the VIOP. The VIOP is then commanded in a timed loop to calculate the frequency of the VIOP 68020 processor clock. The test uses the VIOP line clock interrupt as a time base to calculate the microprocessor clock speed. The VIOP reports to the SPU the timed count value as well as the state of the clock select bit in the VIOP Miscellaneous Diagnostic Register.

The SPU then calculates the MHz value of the VIOP microprocessor clock and prints the value on the screen. The SPU also checks the state of the reported VIOP clock state select bit against what it should be. After nominal clocks are verified, each selected VIOP is set up to run from its margin clock oscillator, and the test sequence is repeated. On exiting from this subtest, the clock selection state for each VIOP is restored to its original state.

Subtest 251, VIOP Cache Buffer Tag

Subtest 251 verifies the VIOP cache buffer tags. Various cache accesses are performed to cause all the buffer tag RAMs to be tested for address uniqueness. As each tag is set, it is checked to verify that the correct tag is set and that no other tag is affected.

Subtest 261, Parity Checker

Subtest 261 verifies the ability of the VIOP to force various parity errors and recover from those errors. The Miscellaneous Diagnostic Register contains the following three special control bits that allow specific parity errors to be generated:

- Force Tag Parity Error Bit
- Force Address Parity Error Bit
- Force Cache Parity Error Bit

The subtest sets the Force Tag Parity Error Bit and verifies that accessing a cache window causes a 68020 bus error and a cache error interrupt. The Cache Error Log is also checked to see that the Force Tag Parity Error Bit is set. The error is cleared and another window access is performed to verify that all the cache errors are cleared.

The same technique is used to test the Force Address Parity Error Bit. The subtest verifies that cache error is generated and the Cache Error Log register reports an address parity error.

The Force Cache Parity Error bit causes a bad PBUS header to be generated and causes a PBUS bus error. The subtest sets this Force Cache Parity Error bit, verifies that a PBUS error interrupt is generated, and checks that the PBUS Error Log reports a PBUS bus error.

Class 3 Subtests

Class 3 subtests verify the functionality of the VIOP cache memory. The current subtests verify the cache in accelerated mode, normal mode, and in bypass mode. Also included is a test of the VIOP cache protection features with respect to VME controller accesses.

Table io5000–6, Class 3 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
300	VIOP Cache Accelerate Read	1:48
301	VIOP Cache Accelerate Write	2:46
302	VIOP Cache Bypass Read	4:04
303	VIOP Cache Bypass Write	3:50
304	VIOP Cache Protection	:30
310	VIOP Cache Test of Dirty Bytes in Longwords	:37
311	VIOP Cache Test of Dirty Longwords in a Buffer	1:15
312	VIOP Cache Test of Dirty Buffers in a Page	:36

Subtest 300, VIOP Cache Accelerate Read

First, subtest 300 sets the accelerate bit in the PMAP register. Then it sets the PMAP register that logically follows the window under test to the nonaccelerate, nonbypass mode.

The VIOP slot number is used to index into a table in main memory that contains patterns and pointers to main memory, which are used to test the accelerate function. The SPU initializes the table before the accelerate test command is given to the VIOP(s). The table is accessed through the nonaccelerated PMAP register as described in the previous paragraph. The table has checksums and a VIOP identification that are checked to ensure the integrity of the data.

Using the information from the table, the test checks the PMAP window under test. Before any location in the page under test is referenced, an initial 64 byte pattern corresponding to buffer locations 0 to 3f is initialized to a known pattern through the nonaccelerated window. The pattern used for the first byte in the page is the VIOP slot number plus the page number of the page under test, modulo 256. The test initializes each successive byte to the value of the previous byte plus 1, modulo 256.

Then a loop is entered in which each of the 4,096 bytes in the page is read and checked for valid data. Additionally, each time byte 0 of each of the two cache buffers is read, the PTAG register for the page is checked to ensure the following:

- Accelerate-on reference bit is set
- Loaded bit is set
- Buffer dirty bit is clear
- TAG value and its parity are properly set

Then, if the previous conditions are met, the test uses the nonaccelerated window to negate the current pattern in main memory. The original pattern remains in the cache. The pattern for the next 64 byte group then is initialized through the nonaccelerated window. When byte 1 of a buffer is read, the test checks the following:

- Accelerate-on reference bit is clear
- Loaded bit is set for both buffers

- TAG value for the current buffer has not changed, and the TAG value for the other buffer is properly set

Subtest 301, VIOP Cache Accelerate Write

Subtest 301 initializes the main memory area used for the write test to the negation of the pattern to be written there. The test then uses the sum of the VIOP slot number plus the page number of the page under test, modulo 256, as the pattern for the first byte. Next, it enters a loop into which each of the 4,096 bytes in the page is written, one byte at a time. As each byte is written, the dirty bits for that longword are checked to make sure that they are set to the expected value. The test then checks the PTAG register for valid data. When byte `0x3f` of each buffer is written, the corresponding area of main memory is read through the nonaccelerated window to ensure that the pattern has not yet been written.

Every time byte `0` of a cache buffer is written, beginning with byte `0x40` in the page under test, the PTAG register is checked to verify that the accelerate-on reference bit is set. When byte `1` of a buffer is written, the nonaccelerated window reads main memory to verify that the pattern for the previous 64 byte block is written to memory and to verify that the accelerate-on reference bit resets.

After the last 64 byte block is written, the window under test is flushed so that all data is written to memory. Finally, the test again checks the pattern in the entire 4,096 byte block for integrity through the nonaccelerated window.

Subtest 302, VIOP Cache Bypass Read

Subtest 302 checks each of the windows in the VIOP cache. As in the accelerate read test, this test places the window that logically follows the window under test in the nonaccelerate, nonbypass mode and verifies the operation of the window under test. Then it initializes the main memory area for the bypass test to the negation of the pattern to be written there. It uses the same patterns as those listed for Subtest 300, VIOP Cache Accelerate Read.

For each 4,096 bytes in the window, the test first uses the nonaccelerate window to write a 1 byte pattern to main memory. Then it reads the byte just written through the window under test and verifies the data. Finally, it negates the byte in main memory through the nonbypass window.

Subtest 303, VIOP Cache Bypass Write

Subtest 303, the logical complement of Subtest 302, tests each window in the VIOP cache. It initializes the main memory area used to test the cache to the negation of the pattern that is to be written there. It uses the same pattern described in the cache accelerate tests.

For each of the 4,096 bytes in the window, the test first uses the window under test to write a 1-byte pattern to main memory. Then it uses the nonbypassed window to verify that the pattern was written to main memory.

Subtest 304, VIOP Cache Protection

This subtest tests access protection of the VIOP cache. The 68020 on the VIOP simulates VME controller access into the VIOP cache by placing the cable interfaces into loopback mode and making accesses into VME address space. The VIOP cache protection bits in the PMAP registers determine which VME controllers can access a particular cache window. The subtest tests all of the available protection modes of each cache window for all possible VME controller accesses.

Subtest 310, VIOP Cache Test of Dirty Bytes in Longwords

Subtest 310 verifies that the VIOP cache can correctly update main memory from its cache windows for all possible combinations of dirty bytes in a cache longword.

Subtest 311, VIOP Cache Test of Dirty Longwords in a Buffer

Subtest 311 verifies that the VIOP cache can correctly update main memory from its cache windows for all possible combinations of dirty longwords in a cache buffer.

Subtest 312, VIOP Cache Test of Dirty Buffers in a Page

Subtest 312 verifies that the VIOP cache can correctly update main memory from its cache windows for all possible combinations of dirty buffers in a cache page.

Class 4 Subtests

Class 4 includes only the PBUS interrupt test. Other interrupts are tested in various other tests, such as the Subtest 101, VIOP Self-test.

Table io5000–7, Class 4 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
400	PBUS Interrupt	:02

Subtest 400, PBUS Interrupt

Subtest 400 verifies the ability of the VIOP to request and use the PBUS interrupt bus. The subtest consists of the following three steps:

Step 1: Interrupt Receive Test

In the receive test, all 256 PBUS interrupts are sent by the SPU to the VIOP, one at a time. After each interrupt is sent, the VIOP verifies that only one interrupt was received and that the interrupt was received by the proper group. The group is determined by taking the modulo 4 residue of the interrupt number.

Step 2: Interrupt Transmit Test

In the interrupt transmit test, the VIOP sends the SPU interrupt numbers 8, 9, 10, and 11, the four interrupts that the SPU is capable of receiving. The VIOP verifies that the acknowledge for each interrupt is received and the SPU verifies the reception of the four interrupts.

Step 3: Interrupt Loopback Test

The interrupt loopback test causes all 256 interrupts to be sent and received by the VIOP in each of the four possible groups. Like the receive test, as each interrupt is sent, the VIOP verifies that only one interrupt is received and that the acknowledge is also received.

> **NOTE**
>
> The terms receive and transmit are from the VIOP's point of view.

Class 5 Subtests

Class 5 subtests verify the ability of the 68020 to do accesses to the VMEbus Control Unit (VBCU). VMEbus cable interfaces, interconnecting cables, and the VBCU itself are tested for address and data line functionality. Also the VBCU-forced interrupt capability is exercised.

Table io5000–8, Class 5 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
500	VBCU Cable Pattern	:01
501	VBCU Forced Interrupt	:01

Subtest 500, VBCU Cable Pattern

Subtest 500 verifies continuity of the VBCU cable address and data lines. The VBCU is set into pattern test mode and accesses are performed to test the cable with a walking '1's and '0's pattern. The VBCU address save register is used to read back the last VME address accessed to verify the address lines.

Subtest 501, VBCU Forced Interrupt

Subtest 501 uses the VBCU Forced Interrupt Register to test the ability of the VBCU to interrupt the 68020. The subtest forces all eight available interrupts and checks that the correct interrupt vector is received for each one for interrupt levels 1 and 3.

Class 6 Subtests

Class 6 subtests uses the VBCU analog to digital converters to measure the VME chassis power supplies. The supplies are tested in normal mode and the +5 supply is also tested under margin conditions.

Table io5000–9, Class 6 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
600	VMEbus Voltage	:01
601	VME Chassis Power Supply Margin	:01

Subtest 600, VMEbus Voltage

Subtest 600 reads and checks the four voltages in each of the VMEbuses for out-of-tolerance conditions. The voltages and tolerances for a VMEbus are listed in the following table:

Table io5000–10, VMEbus Voltages and Tolerances

VOLTAGE	MINIMUM TOLERANCE	MAXIMUM TOLERANCE
+12.10	+11.40	+12.60
+05.10	+04.75	+05.25
-12.10	-12.60	-11.40

Subtest 601, VME Chassis Power Supply Margin

Subtest 601 performs the same voltage test as Subtest 600 on the VME chassis +5 volt supply for upper and lower voltage margins. On some VME chassis, the margin capability is disabled by a jumper on the VME backplane. In this case, the subtest prints the message:

```
Subtest 600 VME 0 not tested - margining disabled
```

idc4000

Integrated Disk Channel Test

Overview

Information needed to document this test was unavailable at press time. The next release of this manual will include this test description.

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dev4100

Multibus SMD Disk Test

Overview

The *dev4100* test checks the Xylogics 450/451 controller and any attached Storage Module Drive (SMD) devices.

Prerequisites and Required Equipment

This test is dependent on the existence and correctness of the SPU disk file */mnt/bin/lib/DB_diskfmt*. Refer to the section "Disk Parameters File, *DB_diskfmt* Description" in this test description for more information about this file.

The test requires the system configuration in one of the next two tables depending on the type of machine under test.

Table dev4100–1, Hardware Requirements (C1, C120)

ITEM	MINIMUM	MAXIMUM
Xylogics 450/451 controller	1	12
SMD device	1	12
Input/output processor (IOP)	1	5
Multibus card cage	1	10 (2/IOP)
Service processor unit (SPU)	1	1
Multibus control unit (MBCU)	1	12
Memory control unit (MCU)	1	1
Memory array unit (MAU)	4MB	System limit

Table dev4100–2, Hardware Requirements (C200 Series)

ITEM	MINIMUM	MAXIMUM
Xylogics 450/451 controller	1	12
SMD device	1	12
Input/output processor (IOP)	1	12
Multibus card cage	1	12
Service processor unit (SP2)	1	1
Multibus control unit (MBCU)	1	12
Memory system (one odd, one even)	1	System Limit
Peripheral interface adapter (PIA)	1	4
CPU utilities (CPX)	1	1

If a SMD is not available, only some of the Class 1 subtests can be run to check a Xylogics

450/451 controller. (Refer to Table dev4100-5, Class 1 Subtests in this chapter for the Class 1 subtests that can be executed without a SMD device.)

Test Invocation

The *dev4100* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4100* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4100–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4100 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4100** executes all *dev4100* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the *-c* or *-s* options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4100–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4100 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

To receive help or information during test parameter entry, enter one of the following characters followed by RETURN:

Table dev4100–3, Getting Help During Test Parameter Entry

CHARACTER	DESCRIPTION
?	Provides the help information
d	Displays *diskfmt* file containing the drive parameters
e	Displays drive entries you have made
h	Provides help for a specific prompt
i	Displays the */ioconfig* file

After the desired help information is displayed, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** figure illustrates *all* prompts that can be asked during test parameter input. However, some prompts may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed during testing may not correspond to those shown in the figure, as the questions illustrated are examples only.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

The test parameter prompts are repeated and explained in the following paragraphs:

```
Are writes to disks allowed [y,n]                    (n) ->
```

Enter **y** to allow writes to the selected disks. The test itself screens all commands before they are allowed to execute and inhibits any operations which are data destructive regardless of whether the write protect switch on the drive is set or not.

```
Number of errors allowed per device each subtest
[0-65535]                                            (0) ->
```

Enter the number of errors that can occur and still allow a device to continue. For instance, if **3** is entered, a device can have 0-3 errors and continue running. On the fourth error, the device stops and is not restarted for the duration of the test.

```
Number of devices failed after which test aborts
[0-65535]                                            (0) ->
```

Each time a unit fails (exceeds the subtest error limit), a count of the number of failed devices is incremented. When a controller fails, the count is incremented for the controller and for each active drive on the controller. If this count exceeds the number of devices specified at this prompt, the entire *dev4100* test aborts.

```
Run subtest 112 to check Attn/Ack [y,n]              (n) ->
```

> **NOTE**
>
> This feature is not used in the OS driver, so this feature does not affect the use of the controller; therefore, enter **n**. Refer to Subtest 112, Verify Attention Request/Acknowledge for more information.

Enter **y** to execute Subtest 112, Verify Attention Request/Acknowledge. Subtest 112 verifies an active controller will stop processing and acknowledge an attention request which allows the CCU driver to add or remove Input/Output Parameter Blocks (IOPBs) from an active chain. Enter **n** and Subtest 112 will not be executed.

Figure dev4100–3, Test Parameter Menu

```
                    ENTER TEST PARAMETERS
       []     Encloses allowed input ranges or values
       ()     Encloses the default value
       ^      Returns to the previous prompt
       :nn    Returns to the prompt # nn
       :      Returns to the first unsatisfied prompt
       :?     Reviews previous entries
?      Prints an additional help menu
 1:  Are writes to disks allowed [y,n]              (n) ->
 2:  Number of errors allowed per device each subtest
    [0-65535]                                       (0) ->
 3:  Number of devices failed after which test aborts
    [0-65535]                                       (0) ->
 4:  Run subtest 112 to check Attn/Ack [y,n]        (n) ->
 5:  Ioconfig file []                        (/ioconfig) ->
                PERIPHERAL CONFIGURATION DATA[1]
      CCU    Chassis  Type      CSR    Int  Unit  TYPE
     -------- -------  --------  -----  ---  ----  --------
 1)  iop  4     0   DKC-001   0x3f0    2     0    DKD-008
 2)  iop  4     0   DKC-001   0x3f0    2     1    DKD-005
 3)  iop  4     0   DKC-001   0x3f0    2     1    DKD-005
 4)  iop  4     0   DKC-001   0x3f0    2     0    DKD-008
 5)  iop  4     0   DKC-001   0x3f0    2     1    DKD-008
Enter device 99 to begin user-defined configurations or 0 to end selection
 6:  Device selection [0,1-5,99]                   (0) ->
 7:  Already formatted [y,n]                       (y) ->
Enter device 99 to begin user-defined configurations or 0 to end selection
 8: Device selection [0,1-5,99]                    (0) ->
Enter IOP -1 to end user-defined configurations
 9:  IOP [0,3-7]                                    () ->
10:  Multibus Chassis [0-3]                        (0) ->
11:  Controller Offset in Multibus [0x0-0xfff]
                                                (0x3f0) ->
12:  Interrupt number [0-7]                        (2) ->
13:  Unit number [0-3]                             (0) ->
14:  Drive name []                          (DKD-005) ->[2]
15:  Already formatted [y,n]                       (y) ->
Enter IOP -1 to end user-defined configurations
16:  IOP [0,3-7]                                   () ->
17:  Enter OK, or :NN to return to question NN [OK]
                                                  (OK) ->
          ********** WARNING!  ***********
        THIS TEST IS POTENTIALLY DATA DESTRUCTIVE!
        IF YOU CONTINUE, DATA COULD BE LOST!
Do you want to continue [yn]      ->
```

[1] The configuration data is only displayed once; to display it again, type **i** (RETURN) at any prompt during test parameter query.

[2] The drive name must match with a drive in the disk parameters file (*/mnt/bin/lib/DB_diskfmt*). To display the *DB_diskfmt* file, type **d** (RETURN) at any prompt.

```
Ioconfig file []                                    (/ioconfig) ->
```

This test query allows selection of a file that contains peripheral device descriptions. The default displays the system's configuration file. To display an I/O configuration file previously created, enter the filename. The configuration file is then displayed. (A relative or absolute path may be specified.)

If drives are to be tested with other than the expected configuration, a new I/O configuration file may be created. As an alternative, nonstandard configurations may be entered by responding to the user-defined configuration test parameters (questions 9-16 as shown in Figure dev4100-3, Test Parameter Menu). Then the drive and/or controller does not have to be defined in an I/O configuration file. Drives from an I/O configuration file can be selected and also drives can be defined with user-defined configurations.

```
Device selection [0, 1-5, 99]                              (0) ->
```

Enter the number of the device to be tested. Only one device can be selected with each device selection prompt. A total of 12 devices can be selected in any order.

If **99** is entered, the following four test parameters do not display. Instead, the user-defined prompts are displayed, beginning with prompt `IOP [0, 3-7]`. If **0** is entered, user selection of devices terminates and the prompt `Enter OK` is displayed.

```
Already formatted [y,n]                                    (y) ->
```

If **y** is entered the drive must be formatted prior to running *dev4100* Class 1 subtests.

```
Device selection [0, 1-5, 99]                              (0) ->
```

Enter the number of another device from the I/O configuration file. If **0** is entered, selection of devices is terminated. If **99** is entered, prompts are displayed that allow configurations to be defined that do not exist in the I/O configuration file.

```
IOP [0, 3-7]                                               () ->
```

This prompt begins the queries for user-defined drives; additional prompts are displayed requesting hardware configuration information. Enter the CCU slot number for the desired IOP or **-1** to terminate device selection. On a C1 or C120, the valid range of IOP numbers is 3-7. On a C200 Series machine, the valid range for IOP numbers is 0-3.

```
Multibus chassis [0-3]                                     (0) ->
```

Enter the number of the chassis to be tested. (The drive is attached to a controller which is in a Multibus chassis.)

```
Controller Offset in Multibus [0x0-0xfff]
                                                       (0x3f0) ->
```

Enter the low-order 12 bits of the controller's address within the Multibus.

```
Interrupt number [0-7]                                    (2) ->
```

Enter the interrupt level of the controller within the Multibus.

```
Unit number [0-3]                                         (0) ->
```

Enter the unit number of the drive to be tested. The unit number entered should also be the unit selected on the drive. (Up to four drives can be attached to one controller; each drive is assigned a unit number which is usually switch selectable on the drive.)

```
Drive name []                                        (DKD-005) ->
```

Enter the drive name. The response to this query must be in the form of DKD-xxx and the name must match one of the drive definitions in the disk parameters file (*/mnt/bin/lib/DB_diskfmt*).

```
Already formatted [y,n]                                   (y) ->
```

Enter **y** if the drive has been previously formatted by the utility *diskfmt*; otherwise, enter **n**. If **y** is entered, time is saved because the subtests do not need to format the disk before starting read and write I/O operations.

```
IOP [0,3-7]                                               (0) ->
```

Enter the CCU slot number for the desired IOP to set up test parameters for another user-defined drive; otherwise, enter a **-1** or RETURN to terminate device selection. On a C1 or C120, the valid range for IOP numbers is 3-7. On a C200 Series machine, the valid range for IOP numbers is 0-3.

```
Enter OK, or :NN to return  to question NN [OK]
                                                      (OK) ->
```

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

```
Do you want to continue [yn]                              ->
```

Enter RETURN to begin test execution, or enter **n** to abort the *dev4100* test. When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure dev4100–4, Sample Test Parameter Summary

```
                TEST PARAMETER SUMMARY

Are writes to disks allowed                                :
Number of errors allowed per device each subtest           : 0
Number of devices failed after which test aborts           : 0
Run subtest 112 to check Attn/Ack                          :
Ioconfig file                                              : /ioconfig
Enter OK, or :NN to return to question NN                  : OK

                        DRIVE CONFIGURATION DATA

         IOP Mbus Mbus  Int   Unit  #    #  Phys  Log Pre-
          #   #   CSR  Level   #   Cyl  Hds  Sec   Sec Fmtd   Name
         --- --- ----- -----  --- ---  ---  ---   --- ---  -------
    1.    4   0  0x3f0   2     0  1024  27   68    67   y    DKD-008
 1000.    4   0  0x3f8   3     1   760  19   60    59   y    DKD-005

Performing sysreset of ccus and memory...
Initializing I/O subsystem and Loading IOP(s)
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

This test contains the following two classes of subtests which are listed in the following table:

Table dev4100–4, *dev4100* Test Classes

CLASS	DESCRIPTION
1	Controller functionality tests
2	Drive functionality tests

Class 1 Subtests

Class 1 subtests exercise all the commands of the Xylogics 450/451 controller to verify its functionality. The subtests contained in *dev4100* are shown in the following table:

Table dev4100–5, Class 1 Subtests

SUBTEST	DESCRIPTION	SMD REQUIRED	WRITE REQUIRED	TIME (minsec)
100	Performs controller reset and checks default drive status for each drive			0:01
101	Executes self-test command			0:01
102	Executes DMA test command			0:01
103	Performs controller buffer write/read commands (max throttle)			0:01
104	Verifies command chaining			0:01
105	Performs NOP command; verifies that specified drives are online	x		0:01
106	Executes set drive size and read drive status commands			0:01
107	Formats a track of diagnostic cylinder and reads track header; uses all interleaves	x	x	0:02
108	Verifies write track headers command; reads back with read track headers command	x	x	0:01
109	Verifies write and read (with verify) commands (all throttle settings)	x	x	0:02
110	Verifies seek command	x		0:01
111	Performs write and read header, data, and ECC command	x	x	0:01
112	Verifies attention request/acknowledge	x		0:02
113	Verifies that controller rejects bad heads, cylinders, sectors, and a bad command	x	x	0:01

Subtest 100, Perform Controller Reset and Read Drive Status Command

Subtest 100 performs a controller reset on each controller and verifies that the reset works by checking the address and relocation registers of the controller. It also performs a pattern test of these registers with walking '0's and '1's patterns.

Subtest 101, Execute Self-test Command

Subtest 101 executes each controller's self-test by first using polling, then using interrupts in place of polling, and repeating the self-test.

Subtest 102, Execute DMA Test Command

Subtest 102 executes a Direct Memory Access (DMA) test, transferring patterns that check every data line to each controller. Each pattern consists of one data bit turned on, while other bits are set to zero. The test causes the *on* bit to rotate through each data bit to verify that each bit can assume an *on* and *off* state and to check that no data bit affects other data bits.

Subtest 103, Perform Controller Write/Read

Subtest 103 performs a 512 byte write to and read from the memory buffer in each controller to verify that the *load* and *dump* buffer commands work. During testing, the throttle setting is set to 128 words per DMA burst, which is the maximum allowed. The subtest writes and verifies a `0x55` pattern followed by a second write and verify using a `0xAA` pattern.

Subtest 104, Verify Command Chaining

Subtest 104 verifies that command chaining works by chaining a write followed by a read of a 512 byte buffer within the controller. If other controllers are available, then this subtest executes until all controllers are checked for chaining. The test performs two write/read sequences per controller. The first write uses a repeating pattern of `0x55`; the second, a `0xAA` pattern.

Subtest 105, Perform NOP Command

Subtest 105 performs a *NOP* command on all drives selected via the test parameter queries. The *NOP* command selects a drive, checks for drive ready, and then de-selects the drive. If any of the selected drives show up as not ready, this test fails.

Subtest 106, Execute Set Drive Size and Read Drive Status Commands

Subtest 106 performs a *read drive status* command on all drives of every controller. It uses the *set drive size* and *read drive status* commands to verify that the configuration can be changed.

Subtest 107, Verify Format and Read Track Headers Commands

Subtest 107 formats track 0 on the diagnostic cylinder and read verifies the success of the format by performing a *read track headers* command. The test checks this information to verify an interleave of 1 and the correct number of headers. Then the test attempts interleaves of 2, 3, 4, etc., through an interleave of 16 and verifies the interleave was formatted correctly.

Subtest 108, Verify Write Track Headers Command

Subtest 108 verifies the *write track headers* command by performing a *read track headers* on track 1 of the diagnostic cylinder. It then writes the headers back out with all head sector numbers set to 0. The test verifies the changed headers by performing another *read track headers.*

Subtest 109, Verify Write and Read Commands

Subtest 109 ensures that the *write* and *read* commands work. This subtest first identifies two consecutive sectors on track 2 of the diagnostic cylinder. Then it writes and read verifies the following data:

Table dev4100–6, Subtest 109, Write and Read Data

SECTOR (of the two chosen)	PATTERN	SECTOR
1st	0x55	Single sector I/O
1st	0xAA	Single sector I/O
Both	0x55	Multisector I/O
Both	0xAA	Multisector I/O

Subtest 110, Verify Seek Command

Subtest 110 verifies the *seek* command completes without error. First it seeks to the diagnostic cylinder and confirms its position by reading track headers. A *seek* is then executed to the maximum cylinder and a *read track headers* is again used to confirm positioning.

> **NOTE**
>
> Although the *seek* command completes without error, this subtest may not detect that the controller did not seek the drive. Although a *read track headers* command is issued after the seek to verify the head is on the correct cylinder, the head may get to that cylinder through the implied seek of the *read track headers* command instead of by the *seek* command. Thus, an error in the *seek* command would not be detected. This also implies that the controller did not update its internal cylinder position when the *seek* command was issued, because, if it had, the implied seek would not occur. For these reasons, it is highly unlikely that this test would fail to detect a seek error.

Subtest 111, Perform Write and Read Header, Data, and ECC

Subtest 111 reads header, data, and Error Correcting Code (ECC) information from each drive and writes it back. Header, data and ECC are known as HDE. Before beginning, it locates two consecutive sectors on track 3 of the diagnostic cylinder. The test writes and read verifies these sectors with test patterns 0x55 and 0xAA, respectively. These sectors are read using the *read HDE* command. It verifies the headers and data fields, and then swaps data and data ECCs between the two sectors. Next, the *write HDE* command writes the sectors back out, and then the test issues the *read HDE* command to read the data back from the two sectors. When the test completes, the data should be in the opposite sectors from where it was originally written.

Subtest 112, Verify Attention Request/Acknowledge

Subtest 112 verifies that the attention request/acknowledge feature of the controller works. This technique is used when the controller driver wants to add parameter blocks onto an already executing chain.

> **NOTE**
>
> This feature does not work at the time of this printing because the controller has a known flaw; therefore, Subtest 112 should not be enabled. It is also not used in the OS driver. If this feature is corrected in the future, this test should be enabled.

The test builds a chain of four *read track headers* commands to each drive on the minimum, maximum, and back to the minimum cylinder to ensure they do not complete before the last two parameter blocks are added to the chain. The last parameter block performs one more minimum-maximum track seek. Once all commands for a drive have completed, all parameter blocks are checked to verify that they completed successfully.

Subtest 113, Verify Controller Reject

Subtest 113 first sends a head address outside the limit the controller is checking; the controller should reject it. Then the test sends a cylinder address outside the drive's range and a sector address outside the controller's limits. The controller should reject these as well.

Class 2 Subtests

Class 2 contains subtests that verify the drive's functionality. These tests verify that the drive can seek, switch heads, read, and reject a bad head or cylinder. The subtests contained in *dev4100* are shown in the following table.

Table dev4100–7, Class 2 Subtests

SUBTEST	DESCRIPTION	SMD REQUIRED	WRITE REQUIRED	TIME (minsec)
200	Verify head switching	x	x	0:02
201	Verify sequential-track seeks	x	x	0:45
202	Perform minimum to maximum track seeks	x		0:10
203	Perform accordion seeks	x		1:15
204	Perform random seeks	x		1:15
205	Verify detect of forced faults (bad cylinder, head, and sector)	x		0:01

Subtest 200, Verify Head Switching

Subtest 200 verifies that the heads switch correctly. The test formats all heads on the diagnostic track and then reads them back with a *read track headers* command. It checks the head number in a header on each head and verifies the shift of the headers by one sector per head.

Subtest 201, Verify Sequential Track Seeks

Subtest 201, performs a *read track headers* command on each cylinder to confirm positioning.

Subtest 202, Perform Minimum to Maximum Track Seeks

Subtest 202 performs a *min-to-max* track alternate seek. Special formatting takes places for Class 2 subtests, if necessary, before the main portion of this subtest executes. The seek begins with an implied seek to the minimum track with a *read track headers* command. After the test verifies the cylinder number, a seek to the maximum track is performed using the *read track headers* command. When this cylinder is verified, the seek repeats to minimum and maximum tracks 100 more times with verification at each track. Each seek is an implied seek using the *read track headers* command. The seek then repeats, using the *seek* command with no verification until the seek is complete. To complete the test, the last track is read with a *read track headers* command and positioning is verified.

Subtest 203, Perform Accordion Seeks

Subtest 203 exercises the drive in an accordion seek. The seek starts with a *seek* to the minimum track, maximum track, min+1, max-1, min-2, max-2, etc., until a one-track seek is performed. The *read track headers* command actually issues an implied seek for each seek. The test verifies the seek by checking one of the headers just read. The accordion seek then repeats using the *seek* command and no verification. After the last seek is performed, a *read track headers* command is performed to verify that the final positioning is correct. The test chains commands for every drive, if allowed.

Subtest 204, Perform Random Seeks

Subtest 204 performs 1000 random seeks within the specified minimum and maximum cylinder. Random numbers are created by initializing C's random number generator with a seed value of 113 and then by calling *rand* for successive numbers. All seeks are implied by the *read track headers* command, which verifies positioning. The test then performs the random seek using the *seek* command with no verification until the seeks are complete. Finally, the test verifies the last cylinder with a *read track headers* command. The test chains commands for every drive, if allowed.

Subtest 205, Verify Detect of Forced Faults

Subtest 205 sends a *set drive size command*, which sets the head and cylinder limits to two greater than the maximum values specified in the file */mnt/bin/lib/DB_diskfmt*. Then the test commands the controller to read a track from a cylinder that is two greater than the maximum. This should result in a seek error. No error may occur if the number of cylinders specified in

/mnt/bin/lib/DB_diskfmt is less than the actual number of cylinders. In this case, an `Expected error did not occur` error is displayed.

Next, the test sets the head to maximum plus 2 and selects the diagnostic cylinder. This generates a write fault. After the write fault, the error does not clear until a drive reset is performed. To verify this, the test performs a read of head 0 of the diagnostic cylinder. A write fault should still occur. Finally, the test resets the drive and reads head 0 again; something other than a write fault should occur.

> **NOTE**
>
> A CDC 9766 drive will fail this test because it reports no error when an attempt to seek two cylinders beyond the defined maximum is made.

Disk Parameters File, *DB_diskfmt* Description

The disk parameters file, */mnt/bin/lib/DB_diskfmt*, contains information about disk drives. This information is required to be able to format/test new drives. Each line in the file contains a number of fields separated by one or more spaces. Comments start with a # in column 1. To add new drives, create a new entry with all the fields defined, and then add the drive to the */ioconfig* file. As of the time of this printing, *DB_diskfmt* contains the following information for all CONVEX machines:

Figure dev4100–5, Contents of the *DB_diskfmt* File

```
# DB_diskfmt - file of disk parameters
# >>>> WARNING - DO NOT USE 'diskfmt' TO FORMAT! It is no longer compatible
# >>>>           with the CONVEX FORMAT! Instead, format MBUS-attached drives
# >>>>           with 'dev4110' and VME-attached drives with 'dev5130'.
# KEY FOR DRIVE NAMES (unformatted capacity is given in parentheses):
#  Name          Description           Name          Description
# DKD-001       Fujitsu Eagle (452MB) DKD-008,208  NEC 2363 (1080MB)
# DKD-002       CDC 9766 (300MB)      DKD-214      Hitachi DK514-38 (356MB)
# DKD-005,206   NEC 2352 (500MB)
#------- XYLOGICS 450/451 SMD CONTROLLER (MBUS) -------
#  a    b    c   d  e  f    g     h    i j k  l  m   n    o  p
DKD-001 2  842 20 46 45 4800 28160 1 0 1  0  0  smd mfm y
DKD-002 0  823 19 32 31 5040 20160 1 0 1  0  0  smd mfm y
DKD-005 0  760 19 60 59 4832 36288 1 0 1  0  0  smd 2-7 y
DKD-008 1 1024 27 68 67 4816 40960 1 0 1  0  0  smd 2-7 y
#------- INTERPHASE 4201 ESDI CONTROLLER (VME) --------
#  a    b    c   d  e  f    g     h    i j k  l  m   n    o  p
DKD-214 0  903 14 51 50 4736 30240 5 5 1  8  8 esdi 2-7 n
#------- INTERPHASE 4200 SMD CONTROLLER (VME) ---------
#  a    b    c   d  e  f    g     h    i j k  l  m   n    o  p
DKD-206 0  760 19 60 59 4832 36288 5 4 1 12 12  smd 2-7 n
DKD-208 0 1024 27 68 67 4816 40960 5 6 1 16 12  smd 2-7 n
# LEGEND:
# a - drive name                Must be DKD-0XX for Multibus and DKD-2XX for
#                               VMEbus
# b - disk type                 For Xylogics controller
# c - # of cylinders
# d - # of heads
# e - # of physical sectors     Number of actual sectors excluding runt
# f - # of logical sectors      Number of physical sectors (e) minus number of
#                               spares
# g - bits per sector           Number of bits between sector pulses
# h - bytes per track           Total number of unformatted bytes per track
# i - skew                      Sector offset from one head to the next
#                               Must be 1 when using Xylogics 450/451 cntlr
# j - # of relocation tracks    .5% of number of cylinders (c). Raise
#                               fractional part to next higher whole number.
#                               Ignored by dev4110 (Multibus formatter)
# k - interleave                sector separation between consecutive sectors
#                               Currently must be 1 for Xylogics 450/451 cntlr
# l - gap 1 size                Number of halfwords in gap before header
#                               (2 bytes per halfword)
#                               Ignored by dev4110 (Multibus formatter)
# m - gap 2 size                Number of halfwords in gap following header
#                               (2 bytes per halfword)
#                               Ignored by dev4110 (Multibus formatter)
# n - drive interface           Used to determine how to read manufacturer's
#                               defect map.  Currently, smd or esdi
#                               Ignored by dev4110 (Multibus formatter)
# o - data encoding scheme      Way data is encoded on the media. Used to
#                               select patterns for pattern test.
#                               Currently mfm, 2-7 or 1-7
# p - Are spares interleaved    For Xylogics, 'y'. For Interphase, 'n'.
```

Diagnostic Cylinder Description

The diagnostic cylinder is located on the first full cylinder preceding the sector forwarding area. Cylinder 840 is the diagnostic cylinder on a Fujitsu Eagle drive, and cylinder 820 is the diagnostic cylinder on a CDC SMD drive.

Each track of the cylinder is independent of the other tracks since there is a "table of contents" stored at sector 0 of each track This table describes what is stored on the remainder of that track. The format of this table is shown below:

Figure dev4100–6, Diagnostic Cylinder Table of Contents Format

```
/* ------------------------------------------------------------------ *
 *              Diagnostic Cylinder Definitions                       *
 * ------------------------------------------------------------------ */
#define NOT_USED        0x00000000      /* position in tbl not used     */
#define NO_HDR          0x00000001      /* this sectors header deleted  */
#define TBL_CONT        0x00000002      /* sector contains tbl of cntnts*/
#define ECC_ERR         0x00000003      /* sector written with bad ecc  */
#define PATTERN         0x00000004      /* sector written with pattern  */

 struct   tbl_cont {
    int   magic_nbr;            /* identifies this as a table of contents */
    int   version;              /* version number of this table */
    int   cyltksc;              /* sector header for this sector*/
    struct {
         int   sec_cont;         /* defines contents of corresponding sector */
         int   pattern;          /* pattern or mask used to verify contents  */
    } sec_tbl[62];
    int   checksum;             /* arithmetic tally of all the above fields */
 };
```

Each track on the cylinder is formatted in such a way that sector 0 is always on the track; sector 0 is written and verified without error when the drive is formatted.

The first field in the table contains the magic number 0x84101500. If this number is not present in the first position of a table, then someone has altered the diagnostic cylinder.

The second field in the table contains the version number. This number is an ordinal number starting with one and increasing as needed. Its purpose is to allow some measure of compatibility of newer diagnostic cylinders with older software. This number is checked if an unknown entry in the sector table (sec_tbl) is encountered. If the version number in the table is greater than the version number of the software, the diagnostic cylinder is assumed to have been formatted with a newer revision of software, and the opcode in the sector table is new to the older software. Therefore, the software is not familiar with the opcode, and the entry in the sec_tbl is ignored.

The next field in the table contains a copy of the sector header (cyltksc) for the table of contents.

The next field in the table contains the sector table (sec_tbl). This table describes what is stored on the rest of the sectors in this track. The sector table consists of 62 entries of 2 int's. Each entry (0 - 61) in this table, corresponds to a sector (0 - 61) on the track. The first position in

each entry is the sector contents (sec_cont) field. If the track has more than 62 sectors, the extra sectors are not used or checked by current software. The following table describes what is currently defined:

Table dev4100–8, Defined Values for Sector Contents Field

FIELD	DESCRIPTION
NOT_USED	This sector has not been initialized and should not be checked.
NO_HDR	When this sector is read, the controller should return a 0x05 sector not found error.
TBL_CONT	This sector contains a copy of the table of contents.
ECC_ERROR	This sector contains a copy of the table of contents that has been corrupted to give some form of ECC error. The pattern field contains a mask which may be xor'ed with the magic number field to correct the error. If the mask contains 11 or fewer one bits, the controller should report a soft ECC error when this sector is read. If the mask contains more than 11 one bits, the error reported should be a hard ECC error.
PATTERN	This sector has been filled with the data contained in the pattern field. No errors should be encountered when the sector is read.

The last field in the table of contents is a checksum. This is an arithmetic tally of all the bytes in the table of contents. This value is checked before any of the data in the table of contents is used.

Error Codes

The *dev4100* test reports controller and device errors in a standard format. However, if additional data is available at the time of the error, it reports that data also. The basic format for the errors is:

dev4100 ERROR (Err) ccu/mb/csr/d=c/m/rrr/d Err_desc

where:

(*Err*) Identifies the error code associated with the description.

Err_desc Describes the type of error that occurred.

c Gives the CCU slot number for the IOP.

m Is the Multibus chassis number.

rrr Gives the control and status register address (CRS), which identifies the board.

d Specifies the device number. Each device begins at 0 with additional drives of the same type being numbered 1, 2, and 3. The number 4 indicates the controller itself was under test.

If no device is associated with the error, then the controller and device information does not appear in the error message.

Additional data may also be reported on a second line (depending on the type of error). For example, the format for data compare errors is:

Cyl:dddd Hd:dd

The following format appears when errors involve *write*, *read*, *read* and *write HDE*, *read* and *write track headers*, or *seek* commands (depending on the error, the sector number or number of seeks may not appear in the error message):

Cyl:dddd Hd:dd Sect:ddd Disp:ddd Exp:hhhh Act:hhhh #Seeks:d

where:

Cyl:dddd Specifies the position of heads on the drive.

Hd:dd Identifies the head selected.

Disp:ddd Identifies number of bytes from the beginning of the sector (data compare errors only).

Exp:hhhh Specifies the expected value (data compares errors only).

Act:hhhh Specifies the actual value (data compares errors only).

Sect:ddd Indicates the sector where the error occurred.

 # Seeks:d Identifies the number of seeks executed.

Error Messages

During execution, if the error limit is exceeded, the test aborts and displays:

```
Subtest Termination in Progress
```

For normal test completion, a message displays in the following format:

```
************ Test started Tue Mar 11 10:30:25 1986
************ Test ended   Tue Mar 11 10:34:15 1986

dev4100 Termination complete.
```

During execution, *dev4100* outputs error messages from the controller, IOP, disk device sequencer, and device subtests. The following sections describe these errors.

Controller Error Messages

> **NOTE**
>
> In the following error messages, IOPB represents Input Output Parameter Block.

0x00 IOPB completed without error
The controller completed the command successfully without an error.

0x01 Interrupt pending
The controller attempted an operation with a previous interrupt still pending. While an interrupt is pending, only the following operations are permitted: interrupt reset, update IOPB, controller reset, or error reset.

0x03 Attempt to write to reg. while busy
The IOP attempted a register write while controller busy is set. When the controller is busy, only bits 2 and 4 of the control and status register (CSR) have write access.

0x04 IOPB not completed within two seconds
The controller did not complete the input/output parameter block within two seconds.

0x05 Header not found
The controller cannot locate the requested sector. Any one of the following could cause this error:

- The actual number of physical sectors in the drive exceeds the maximum number of sectors plus 5. For example, if the controller searches 37 (32 + 5) sectors and the drive has 47 actual sectors, the controller may not compare 10 sectors for valid headers. (The controller compares headers for the maximum number of sectors plus 5.)
- The header the controller finds does not match the header ECC.
- The requested drive type and the drive type contained in the header do not match.
- A media defect may be in the header area.

0x06 Hard ECC error
This error only occurs on a *read* command when the controller detects a data error in the data field longer than 11 bits or when the ECC mode is disabled.

0x07 Bad cylinder from host
The IOP specified a cylinder address greater than the maximum cylinder number allowed.

0x0a Bad sector from host
This message indicates that the IOP specified a sector address greater than the maximum sector number allowed. Verify the maximum sector parameter for this drive type; retry the IOP operation.

0x0d Runt sector too small to write header
Either the last sector or all the sectors are too small to write a complete header. Verify the drive sector switches.

0x0e Memory failed to respond to DMA

This message means that the memory address by the controller failed to respond. The microprocessor provides a 10 millisecond timeout for the DMA sequencer to perform up to 128 transfers. When the timer interrupts, the controller verifies whether it is a bus master. A slave acknowledge error occurs if it is a bus master; a disk sequencer errors occurs when it is not a bus master. Verify the memory address or memory itself; retry the operation.

0x12 Header cylinder or head is incorrect

The cylinder or head address read from the disk does not match the IOPB cylinder and head address bytes.

This error occurs when the disk drive fails to seek to the correct cylinder. Another condition that causes this error is a corrupted disk format. Reformat the disk and retry the operation. In addition, if the head byte written on the disk does not match the selected head address, this error occurs. This indicates that there is a bad format or hardware problem.

0x13 Seek error was corrected by cntlr

The controller encountered a *seek* error. When the controller encounters a *seek* error, it automatically recalibrates the disk drive, clears the error, and completes the *seek*.

0x14 Write-protected disk

The controller attempted a *write* operation on a drive that is write-protected. First remove the write-protect and then retry the *write* operation.

0x16 Drive is not ready or faulted

This error indicates that the selected drive is not ready or possibly faulted. Any one of the following conditions can cause the problem:

- ALCO signal on the multibus backplane connector is low.
- Bad or improperly connected cable.
- Drive not up-to-speed or hardware error.
- Dual port access many not have been granted.
- No drive of the specified unit number is connected to the controller.

0x17 Bad sector count of 0 from host

This message indicates that the IOP issued the controller an IOPB with a sector count of zero. All data transfer operations require a positive sector count.

0x18 Drive reported a fault condition

This error messages indicates that a fault exists in the selected drive.

0x19 Bad sector size from host

The controller cannot write the header and data fields because the drive sectoring does not allow enough room. Any of the following conditions can cause this error to occur:

- The runt sector is too small.
- The drive contains more sectors than the number of specified data sectors plus five.
- Although the last sector is too small to be a data sector, it is included in the specified maximum sector. Either adjust the drive to include more sectors or the drive type (*DB_diskfmt*) to include fewer sectors.

0x1a Self-test A failed
Either the microprocessor or its internal RAM failed diagnostics.

0x1b Self-test B failed
This message indicates that either the microprocessor or header shift register failed diagnostics.

0x1c Self-test C failed
The buffer RAM failed diagnostics.

0x1e Correctable ECC error
The controller detected a correctable 11-bit (or less) error in the data field of the correct sector during a *read* in ECC mode 0.

0x1f Illegal ECC Mode used by Cntlr
During the transfer, the controller corrected one or more ECC errors in ECC mode 2, which should never be used as it does not work correctly in our configuration.

0x20 Bad head from host
The IOP specified a head address greater than the maximum head address allowed, which indicates a malfunctioning controller.

0x21 Disk sequencer error
This message indicates that the disk sequencer did not finish its operation within the allotted time. This can be caused by any of the following factors:

- The controller did not receive the servo clock signal from the selected drive. Check the cable connection.
- The controller is not receiving any read data from the selected drive. Check the cable.
- The Multibus may be preventing the controller from gaining proper access to memory.

0x25 Seek error
The IOP specified a cylinder address greater than the drive maximum or specified a head beyond that supported by the drive. Verify the drive parameters for the drive type tested.

0x3f Dual port drive already connected
The controller attempted to select a dual port drive which was connected to another controller. Since dual part drives are not supported, this error should never occur.

Device Subtest Error Messages

0x40 Bad block table is full
The bad block table can hold a maximum of 639 sectors. It is extremely unlikely that this table would ever fill up so it is much more likely that the bad block table is bad. In other words, the count of the number of used entries that is stored in the table is bad. This error sometimes occurs when a disk has been only partially formatted (headers are there and pattern-test data but no bad block table exists).

0x41 Bad sector not in Bad Block Table

A header not found occurred on a track which usually means the sector has been relocated. However, the sector was not found in the Bad Block Table. This may be due to a disk being only partially formatted.

0x42 No consecutive sectors found

The HDE subtest requires that two consecutive sectors exist on head 3 of the diagnostic cylinder. This error occurs if these headers are not found.

0x47 Bad parm to calc_cyl

This indicates a bug in the software. Please report it.

0x48 Bad parm to calc_hd

This indicates a bug in the software. Please report it.

0x49 Bad parm to calc_sec

This indicates a bug in the software. Please report it.

0x4a IOP print utility memory error

The print utility, prtlog_init, was unable to allocate main memory needed for prints from the CCU. Try running **mminit** and then retrying the test.

0x4b Device FAILED

The specified device failed this subtest. No more testing will be performed on this device.

0x4c Input parms don't allow write

The specified drive does not allow writes, and a write subtest was selected. The write is inhibited.

0x4d All copies of BBT are bad

There are five copies of the Bad Block Table on the last cylinder of each system-formatted disk. This error occurs when none of them are readable.

0x4e Diag. trk has all bad headers

During creation of the diagnostic cylinder, one of the tracks was found to be unusable because none of the sectors were readable. This error is very serious because it indicates either a major media flaw or a failure of that head to read data.

0x4f Diag. cylinder bad

During test of the diagnostic cylinder, sector zero of each track is read and two integer fields in the sector's data are checked against expected values. If they differ, this error results. This is usually caused by *dev4100* being run followed at some time later by a run of Subtest 103 in *dev4110*. The *dev4100* test writes over the diagnostics data written by Subtest 101 in *dev4110*. This problem is easily fixed by rerunning Subtest 101 in *dev4110*. Then use Subtest 103 in *dev4110* to verify the diagnostic cylinder is okay. If it still fails, then there is a problem writing or reading sectors.

0x50 Bad data compare on diag. cyl

Each track of the diagnostic cylinder has most of the sectors written with known patterns. These sectors are read and a data compare is performed to verify no data degradation or overwrite of this data has occurred. If any of these sectors do not successfully data compare, this error results. This could be caused by running *dev4100* prior to running Subtest 103 of *dev4110*.

0x51 N0 err. Hdr-not-found expected
One sector on each of the tracks of the diagnostic cylinder is deliberately removed so that a header not found error will result. If a header not found does not occur, this error is reported. This could be caused by running *dev4100* prior to running Subtest 103 of *dev4110*.

0x52 Soft ECC error did not occur
Subtest 103 of *dev4110* reports this error. Each track of the diagnostics cylinder has 11 sectors with soft ECC errors written to them. If any of these 11 sectors on each track do not cause the controller to report a soft ECC error, this error is reported.

0x53 Hard ECC error did not occur
Subtest 103 of *dev4110* reports this error. Each track of the diagnostics cylinder has one sector that has data with 12 consecutive bits in error. When this sector is read, it should always cause the controller to report a hard ECC error. If this error does not occur, this error is reported.

0x54 Data compare err on diag cyl
Most sectors on the diagnostic cylinder are written with known data patterns. During the test of the diagnostic cylinder, each sector containing known data is compared. This error occurs if a data compare fails. It may indicate degraded media or a bad head.

IOP Error Messages

0x80 Data compare error
Data read by the IOP did not match the expected data. The IOP performs the following data compares:
0x81 Seek requested with a seek count = 0
SEEK_CNT_ZERO – This indicates a bug in the software. Please report it.

0x82 Format of partial tracks not allowed
FORMAT_SETUP_BAD – This indicates a bug in the software. Please report it.

0x83 No attn acknowledge after attn request
NO_ATTN_ACK – This results when the controller is started on a chain of commands and then an attempt to get the attention of the controller in the middle of execution of the chain fails. This is a known problem with the controller and causes Subtest 112 to fail.

0x84 MBS error attempting to return msg
The IOP was attempting to send a message to the SPU when the MBS I/O subsystem reported an error condition.

0x85 Desired IOPB not in active chain
IOPB_NOT_IN_CHAIN – This is possibly due to a bad controller overwriting the pointer to the next IOPB in a chain. However, any component in the path of data from a controller to main memory is suspect.

0x86 Message received on wrong subqueue
The IOP received a message on a subqueue other than seven.

0x87 Wrong subqueue active and locked
The IOP detects a message on a subqueue other than seven, but the MBS locked the subqueue when a receive was attempted.

0x88 Wrong subqueue active and MBS error
The IOP detects a message on a subqueue other than seven. However, MBS reports an error when a message receive is attempted.

0x89 Wrong subqueue active, error invalid
The IOP detects a message on a subqueue other than seven. However, MBS reports an invalid error code when a message receive is attempted.

0x8a Driver executed for no reason
The Event Governed Operating System (EGOS) brought the IOP driver into execution; the driver found no reason for this action.

0x8b Unexpected soft error from Cntlr
The controller reported one of two soft errors when no soft error was expected. The error is one of the following:

Seek Retry Required	The controller detected a seek error and automatically recovered from the error. Because the bit that allows automatic recovery is not enabled, this error should never occur.
Soft ECC Error Recovered	The controller thinks it automatically corrected an ECC error of eleven bits or less. Because CONVEX does not use this function, this error should never occur.

0x8c Cntlr busy after hard error
After a hard error occurs, the controller goes "not busy" (according to the *Xylogics User's Manual*). In this case, a hard error was detected, and the controller was still busy when a retry was attempted.

0x8d Retry in progress-no active chain
NO_ACTIVE_CHAIN – This indicates a bug in the software. Please report it.

0x8e No attn acknowledge after attn request
Subtest 112 of *dev4100* verifies that, when a chain is actively executing, an attention request to the controller will cause the controller to halt without completing the chain and respond with attention acknowledge. This error indicates that this logic in the controller does not work properly. The Xylogics controller has this problem and will generate this error if Subtest 112 is enabled to run.

0x8f Cntlr not busy after release attn request
The controller is designed so that if busy is set when the attention request is asserted, busy remains set after the release of the attention request bit. If busy goes away, the controller does not meet specifications.

0x90 Cntlr busy after release attn
CNTLR_BUSY_ERR – The controller went not busy when during an attention request and before the controller was restarted. This is okay. However, when the controller's attention was released, the controller was found to be busy. This indicates a bad controller.

0x91 Interrupt occurred—no IOPBs done
The controller sent an interrupt; when the active IOPB chain was scanned, no completed IOPBs were found. This interrupt is not caused by an attention request, which is handled separately.

0x92 EGOS routine wndw_alloc returned 0
An attempt to set up a window to main memory from the IOP failed.

0x93 Task init attempt-error pending
RESPONSE_NEEDED – This indicates a bug in the software. Please report it.

0x94 No cntlr interrupt in 5 seconds
The controller must interrupt the driver within 5 seconds after an IOPB chain is started or a timeout occurs.

0x96 Write/Read error in controller regs
Write/Read test of controller registers failed.

0x97 Cntlr was busy after drive fault
The controller must go not busy after a drive fault. This is checked to ensure the controller is working as specified.

0x98 Cntlr stayed busy after drive reset
The controller is specified as going not busy after a drive reset. If it stays busy, this error is reported.

0x99 Attempting to poll-no active IOPBs
NOTHING_TO_POLL – This indicates a bug in the software. Please report it.

0x9a Finished task but int. state wrong
This indicates a bug in the software. Please report it.

0x9b Controller is not present
An attempt to write to the controller resulted in a BUS error, which implies that no controller is present or the controller is dead.

0x9c Sector interleave or skew error
The track headers were read to verify the format, and the headers were not properly interleaved or skewed.

0x9d Bad cylinder address after seek
A check of headers after *seek* revealed that the headers are on the wrong cylinder.

0x9e Set drive size - bad head or sector
A *read drive status* after setting the drive size in the controller showed that either the head or sector size was incorrectly set.

0x9f Set drive size - bad cylinder
A *read drive status* after setting the drive size in the controller showed that the cylinder size was incorrectly set.

0xa0 Expected error did not occur
Subtest 205 of *dev4100* selects a non-existent cylinder, then a nonexistent head is selected. An expected error had better occur or this error results.

0xa1 Error bit(s) set in cntlr csr
If a single or double error is reported in the command and status register and no other error is indicated, this error is reported.

0xa2 No free IOPBs for retry
NO_FREE_IOPBS – This indicates a bug in the software. Please report it.

Device Sequencer Error Messages

0xc0 MBS error-when SPU receiving a message
The MBS reported an error in attempting to provide the SPU with a message.

0xc1 Timeout because queue locked
The SPU received a message, but all ten attempts to read the message resulted in the error *MBS queue locked* being reported by the MBS.

0xc2 Msg interrupt but no msg found
The SPU attempted ten times to receive a message when an interrupt occurred, but all attempts failed with a *no message* error from the MBS.

0xc3 Bad return code from msg_build
BAD_BUILD_RTN – This indicates a bug in the software. Please report it.

0xc4 Timeout awaiting msg
SPU expected the IOP to send a message, but it did not receive a message. This error message indicates that the controller failed to generate an interrupt when done, or a break exists in the path of the interrupt signal, which prevents it from being detected.

0xc5 Rtn msgs from subq other than 7
The SPU received a message to the wrong subqueue; all messages are expected to arrive on subqueue seven.

0xc6 MBS returned bad error code
A call to an MBS routine returned an error code that was unrecognizable.

0xc7 Block transfer routine failed
A memory to memory transfer failed. Memory may be local or main.

0xc8 Too many devices failed. Failed subtest
This message indicates that the test is terminating because the device failure limit was exceeded.

0xc9 Return msg not of valid type
The SPU received a message, but it was not a device result or system error message.

0xca IOP's queue locked too long
Ten attempts to send a message to the IOP failed, with a locked condition being reported by MBS.

0xcb No room on SPU side for msg
Ten attempts to send a message failed because no messages were available for MBS to use.

0xcc Return msg error
An attempt to send a message from the SPU to the IOP resulted in an MBS error being reported.

0xcd Error while configuring I/O
The IOP returned a configuration message that specified a controller that does not exist.

0xce # active dev on cntlr < 0
BAD_DEV_CNT – This indicates a bug in the software. Please report it.

0xcf Too many controllers specified
The user attempted to select drives on too many controllers. This test's limit is 6. The limit for *dev4110* is 12.

0xd0 IOP echoed msgs when none sent
The SPU received an echo message, but no message had been sent.

0xd1 Bad cntlr # in returned msg
BAD_MSG – This indicates a bug in the software. Please report it.

0xd2 Outstanding msg cnt greater than 0
BAD_MSG_CNT – This indicates a bug in the software. Please report it.

0xd3 No msg err when sending to SPU
A message buffer was requested from MBS on the IOP. No message buffer was available. Try again later.

0xd4 MBS error when sending to SPU
The IOP MBS logic reported back an error condition (catchall for unexpected errors) while attempting to send a message to the SPU from the IOP.

0xd5 Inv. MBS err when sending to SPU
MBS on the IOP reported a non-zero error code that is not defined.

0xd6 MBS locked when sending to SPU
MBS on the IOP will not allow the sending of messages because the semaphore on the SPU process's queue is not being released.

0xd7 IOP driver device is bad
This indicates a bug in the software. Please report it.

0xd8 MBS error during IOP msg recv
The MBS routine that receives messages on the IOP reported that it detected an error. Usually this means that main memory no longer contains valid message queues.

0xd9 MBS queue locked during receive
The SPU attempted to receive a message but its queue was locked too long. Should never happen.

0xda MBS no message available
A message should have been in the queue but when it was checked, there were no messages.

0xdd Processor queue setup failed
PQ_SYSTEM_FAIL – The SPU utility, **pqutil** was unable to initialize the processor queues which are needed for SPU<->CCU communications. This is usually due to main memory not being initialized. Try running **mminit** before the test.

0xde Failed to open window
WNDW_OPEN_ERR – An attempt to open the file */dev/wndw* on the SPU disk failed. See if the file exists and verify it has global write permission.

0xdf Failed to allocate map registers
IOCTL_ERR – An attempt to set up map registers to main memory for access from the SPU has failed. This should never happen. Please report it.

0xe0 IOP load module not found
The file that is to be loaded into the IOP does not exist. The current directory is searched first and then */mnt/test* is searched.

0xe1 Error attempting to load iop
The OS utility */mnt/os/loadccu* returned non-zero when it attempted to load the IOP. The usual cause is that *mminit* or a *sysreset* was not performed prior to running the test.

0xe2 Main memory allocation error
MMALLOC_ERR – An attempt to allocate main memory has failed. Try running **mminit** before rerunning the test.

Subtest 600 voltages does not fail

HSP

dev4110

Multibus SMD Disk Formatter, and Interactive Test

Overview

The *dev4110* test is capable of formatting, verifying the format, and interactively testing up to 12 Storage Module Drives (SMDs) at the same time. It also allows manual input of a Manufacturer's Defect (MD) map before or after a format is performed.

Prerequisites and Required Equipment

The *dev4110* test is dependent on the existence and correctness of the SPU disk file */mnt/bin/lib/DB_diskfmt*. Refer to the section, "Disk Parameters File, *DB_diskfmt* Description" in this test description for more information about this file.

The test requires the system configuration in one of the next two tables depending on the type of machine under test.

Table dev4110–1, Hardware Requirements (C1, C120)

ITEM	MINIMUM	MAXIMUM
Xylogics 450/451 controller	1	12
SMD device	1	12
Input/output processor (IOP)	1	5
Multibus card cage	1	10 (2/IOP)
Service processor unit (SPU)	1	1
Multibus control unit (MBCU)	1	12
Memory control unit (MCU)	1	1
Memory array unit (MAU)	4MB	System limit

Table dev4110–2, Hardware Requirements (C200 Series)

ITEM	MINIMUM	MAXIMUM
Xylogics 450/451 controller	1	12
SMD device	1	12
Input/output processor (IOP)	1	12
Multibus card cage	1	12
Service processor unit (SP2)	1	1
Multibus control unit (MBCU)	1	12
Memory system (one odd, one even)	1	System Limit
Peripheral interface adapter (PIA)	1	4
CPU utilities (CPX)	1	1

Test Invocation

The *dev4110* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4110* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4110–1, *dev4110* Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4110 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4110** executes all *dev4110* subtests sequentially except for Class 2 (same as Subtest 200). Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

NOTE

The Class 2 (Subtest 200) Interactive Test is only started by specifying the **-c** or **-s** options. Only the Class 1 subtest runs if only **test dev4110** is entered.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last powerup. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash or hard error), it should be run again. In this case, failure to run *initall* could result in invalid test results. The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. The control stores do not need to be loaded for disk tests. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4110–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4110 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev4110–3, Getting Help During Test Parameter Entry

Character	Description
?	Displays this help menu
d	Displays *DB_diskfmt* file containing the drive parameters
e	Displays entered drive entries
h	Provides help for a specific prompt
i	Displays the */ioconfig* file

After the desired help information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev4110–3, Test Parameter Menu

```
                    ENTER TEST PARAMETERS
        []      Encloses allowed input ranges or values
        ()      Encloses the default value
        ^       Returns to the previous prompt
        :nn     Returns to the prompt # nn
        :       Returns to the first unsatisfied prompt
        :?      Reviews previous entries
?       Prints an additional help menu
 1:  Number of errors allowed per device each subtest
    [0-65535]                                        (0) -> RETURN
 2:  Number of devices failed after which test aborts
    [0-65535]                                       (12) -> RETURN
 3:  Verbosity of test [0-65535]                     (3) -> RETURN
 4:  Ioconfig file []                       (/ioconfig) -> RETURN
                PERIPHERAL CONFIGURATION DATA[1]
      CCU     Chassis  Type     CSR    Int Unit Type
    -------- ------- -------- ------ --- ---- --------
 1) iop  4       0    DKC-001  0x3f0  2   0    DKD-008
 2) iop  4       0    DKC-001  0x3f0  2   1    DKD-005
 3) iop  4       0    DKC-001  0x3f8  2   1    DKD-005
 4) iop  4       0    DKC-001  0x3f8  2   0    DKD-008
 5) iop  4       0    DKC-001  0x3f8  2   1    DKD-008
Enter device 99 to begin user-defined configurations or 0 to end selection
 5:  Device selection [0,1-5,99]                     (0) -> 1 RETURN
 6:  Device selection [0,1-5,99]                     (0) -> 99 RETURN
Enter IOP -1 to end user-defined configurations
 7:  IOP [0,3-7]                                     (0) -> 3 RETURN
 8:  Multibus Chassis [0-3]                          (0) -> RETURN
 9:  Controller Offset in Multibus [0x0-0xfff]
                                                (0x3f0) -> 3f8 RETURN
10:  Interrupt number [0-7]                          (2) -> 3 RETURN
11:  Unit number [0-3]                               (0) -> RETURN
12:  Drive name []                           (DKD-005) ->[2] RETURN
Enter IOP -1 to end user-defined configurations
13:  IOP [0,3-7]                                     (0) -> 1 RETURN
14:  Enter OK, or :NN to return to question NN [OK]
                                                    (OK) -> RETURN

          ********** WARNING! **********
       THIS TEST IS DATA DESTRUCTIVE!
       IF YOU CONTINUE, DATA WILL BE LOST!

************************************************************
* SET WRITE PROTECT ON ALL DRIVES YOU DON'T WANT FORMATTED *
************************************************************
Do you want to continue [yn]  -> y RETURN
```

[1] This information is only displayed once; to display it again, type **i** RETURN at any prompt during test parameter query.

[2] The drive name must match with a drive in the disk parameters file */mnt/bin/lib/DB_diskfmt*). To display the disk parameters file, type **d** RETURN at any prompt.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

The test parameter prompts are repeated and explained in the following paragraphs.

```
Number of errors allowed per device each subtest
[0-65535]                                    (0) ->
```

The number of errors that can occur during a subtest and still allow a device to continue can be specified. For instance, if **3** is entered, a device can have 0-3 errors in any subtest and continue running. On the fourth error, the device stops and is not restarted for the duration of the test. In this example, as long as no more than 3 errors in each subtest occur, the device continues.

> **NOTE**
>
> Subtest 200, Interactive Test reports errors but does not increment the error count when a drive or controller error occurs. In addition, Subtest 100, Input Defects Before Formatting does not affect the error count during pattern test for sector related errors.

```
Number of devices failed after which test aborts
[0-65535]                                   (12) ->
```

Each time a unit fails (exceeds the number of errors allowed each subtest), the count of the number of failed devices is incremented. When a controller fails, the count is incremented for the controller and for each active drive on the controller. If this count exceeds the number of devices specified at this prompt, the entire *dev4110* test aborts. The default number is 12 so the test normally continues even though drives have failed.

> **NOTE**
>
> Drive errors are not counted during the Subtest 200, Interactive Test so failures are not counted during this test.

```
Verbosity of test [0-65535]                 (3) ->
```

The amount of information to be printed can be selected in addition to the standard subtest

execution lines. Choose values of the items to print from the table below and add the values. The sum is the number to enter.

Table dev4110–4, Test Verbosity Levels

VALUE	DESCRIPTION
1	Print summary of all bad sectors found – printed near the end of Subtest 101, Format and Pattern Test.
2	Print each bad sector as it is found in Subtest 101 – may print same sector once for each pattern.
4	Print read of the BBT at startup of Subtest 103, Verify System Format, Subtest 104 Test Diagnostic Cylinder, and Subtest 200, Interactive Test.
8	Print pattern and pass counter in Subtest 200, Interactive Test pattern test. Only the pass counter is normally displayed as an indicator of how far along the test is toward completion.

NOTE

If each bad sector is to be printed as it is found, the following errors are printed.

- 0x05 (header not found)
- 0x06 (Hard ECC error)
- 0x1e (Correctable ECC error)

Any other reported errors than those listed above are countable errors and increment the number of errors per subtest counter. Countable errors are always retried until successful or the number of errors per subtest counter exceeds the number allowed.

The following is an example of verbose output for a value of 1:

Figure dev4110–4, Verbose Output Screen — Level 1

```
SUMMARY OF BAD BLOCKS FOR ccu/mb/csr/d=3/0/3f0/0

 INPUTS THAT WILL NOT BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
         ---------------------- no sectors ----------------------

LOC:  *G=gap  *D=dup  *S=spare  *I=invalid hdr  *B=hdr marked bad

 INPUTS THAT WILL BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
         ---------------------- no sectors ----------------------

LOC:  *G=gap  *D=dup  *S=spare  *I=invalid hdr  *B=hdr marked bad

SUMMARY OF BAD BLOCKS FOR ccu/mb/csr/d=3/0/3f0/1

 INPUTS THAT WILL NOT BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
 ------------------------------ no sectors --------------------------------

LOC:  *G=gap  *D=dup  *S=spare  *I=invalid hdr  *B=hdr marked bad

 INPUTS THAT WILL BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
  22  3   7                  SECC PGM | 372 12   0                  HECC PGM
  51 14  28                  HECC PGM | 523 18   2                  SECC PGM
  77  9  44                  SECC PGM | 544  6  11                   HNF PGM
  78  9  44                   HNF PGM | 591  0   7                  HECC PGM
  79  9  44                  SECC PGM |

LOC:  *G=gap  *D=dup  *S=spare  *I=invalid hdr  *B=hdr marked bad
```

The following is an example of verbose output for a value of 2:

Figure dev4110–5, Verbose Output Screen — Level 2

```
    subtest 101  0:22:14  Pattern 1: 00000000

dev4110 ERROR (0x1E)-ccu/mb/csr/d=3/0/3F0/1 Correctable ECC error
  Cyl:  22 Hd: 3 Sect:  7
 0:23:52

dev4110 ERROR (0x06)-ccu/mb/csr/d=3/0/3F0/1 Hard ECC error
  Cyl:  51 Hd:14 Sect: 28
 0:29:45 Pattern 2: FFFFFFFF

  ----- More errors will probably be reported during other patterns.
  ----- In fact the errors shown above will probably repeat.
```

The following is an example of verbose output for a value of 4:

Figure dev4110–6, Verbose Output Screen — Level 4

```
--------------- BAD BLOCK TABLE READS -----------------
Drive: ccu/mb/csr/d - 3/0/3f0/0
       Reading copy #0 starting at cyl:758 hd:18 sec:34    - failed
       Reading copy #1 starting at cyl:758 hd:18 sec:39    - successful
Drive: ccu/mb/csr/d - 3/0/3f0/1
       Reading copy #0 starting at cyl:758 hd:18 sec:34    - successful
```

The following is an example of verbose output for a value of 8:

Figure dev4110–7, Verbose Output Screen — Level 8

```
(D1;Save)-> p 100 times 0 0 0 to end
pass: 1 pattern: ffffffff
```

With a verbosity setting of 8, the `pass: 1` and the `pattern: ffffffff` line print. Both the pass number and pattern change as the test progresses.

```
Ioconfig file []                              (/ioconfig) ->
```

This prompt allows a file to be chosen that contains peripheral device descriptions. The default displays the system's configuration file. To display an I/O configuration file previously created, enter the filename. Then the configuration file is displayed. (A relative or absolute path may be specified.)

If drives are to be formatted or tested with a configuration other than the expected configuration, a new I/O configuration file may be created. As an alternative, nonstandard configurations may be input by responding to the user-defined configuration test parameters (questions 7-13 in the "Test Parameter Menu" figure). Then the drive and/or controller does not have to be defined in an I/O configuration file. Drives can be selected from an I/O configuration file and then drives can also be defined with user-defined configurations.

```
Device selection [0,1-5,99]                   (0) ->
```

Enter the number of the drive to be tested. One drive can be selected with each prompt for device selection and up to a total of 12 drives can be selected in any order. Refer to the *Hardware Requirements (C1, C120)* table and the *Hardware Requirements (C200 Series)* table for restrictions on hardware configurations.

> **NOTE**
>
> If drives are formatted for system use, the drives should be on separate controllers. Each controller must format drives sequentially so two on one controller doubles the format time.

If **0** is entered, the selection is terminated and the prompt `Enter OK` is displayed. If **99** is entered, the user-defined prompts are displayed, beginning with the following prompt.

```
IOP [0,3-7]                                   (0) ->
```

This prompt begins the user-defined drive prompts, so if all the drives to be used are in the *ioconfig* file, reply RETURN to end the user-defined drive prompts. However, to enter a unique drive configuration (not in the *ioconfig* file), enter the CCU slot number for the desired IOP. Then additional prompts are displayed requesting hardware configuration information.

```
Multibus Chassis [0-3]                        (0) ->
```

Enter the number of the chassis to be tested. (The drive is attached to a controller which is in a Multibus chassis.)

```
Controller Offset in Multibus [0x0-0xfff]
                                              (0x3f0) ->
```

Enter the low-order 12 bits of the controller's address within the Multibus (this address is selected with switches on the controller).

```
Interrupt number [0-7]                    (2) ->
```

Enter the interrupt level of the controller within the Multibus (this is selected with switches on the controller).

```
Unit number [0-3]                         (0) ->
```

Enter the unit number of the drive to be tested. The unit number to enter is also the unit selected on the drive (Up to four drives can be attached to one controller; each drive is assigned a unit number, which is usually switch selectable on the drive). For maximum performance, each drive should be on a separate controller although it is not a requirement.

```
Drive name                              (DKD-005) ->
```

Enter the drive name. The response for this query must be in the form of DKD-xxx and the name must match one of the drive definitions found in the disk parameters file (*/mnt/bin/lib/DB_diskfmt*).

```
IOP [0,3-7]                               (0) ->
```

Enter the CCU slot number for the desired IOP to set up test parameters for another user-defined drive. Enter a **-1** or RETURN to terminate test parameter entry.

```
Enter OK or :NN to return to question NN [OK]
                                          (OK) ->
```

To return to a preceding question at anytime during the test parameter sequence, enter CTRL and RETURN. To return to a specific question and make any further changes, a colon and a question number may be entered, for example, **:3**.

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

```
Do you want to continue [yn]          ->
```

Enter RETURN to begin test execution; or enter **n** to abort the *dev4110* test.

When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure dev4110–8, Sample Test Parameter Summary

```
            TEST PARAMETER SUMMARY

Number of errors allowed per device each subtest      : 0
Number of devices failed after which test aborts      : 12
Verbosity of test                                     : 3
Ioconfig file                                         : /ioconfig
Enter OK, or :NN to return to question NN             : OK

                    DRIVE CONFIGURATION DATA

      IOP MBus MBus  Int   Unit  #    #  Phys  Log
       #   #   CSR  Level   #   Cyl  Hds  Sec  Sec  Name
      --- --- ----- -----  --- ---  ---  ---  ---  -------
   1.  4   0  0x3f0   2     0  1024   27   68   67  DKD-008
1000.  4   0  0x3f8   3     0   760   19   60   59  DKD-005

Performing sysreset of ccus and memory...
Initializing I/O subsystem and Loading IOP(S)...

************************************
* SYSTEM FORMAT IS ABOUT TO START    *
* VERIFY WRITE-PROTECT IS SET ON ANY *
* DRIVES YOU ARE NOT FORMATTING      *
************************************

Then reconfirm that you want to continue    [yn] ->
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev4110* test contains the following two classes of tests.

Table dev4110–5, *dev4110* Test Classes

CLASS	DESCRIPTION
1	System format and verification tests
2	Interactive test

Class 1 Subtests

Class 1 subtests allow a system format to be written to an SMD and to be verified. The proper way to format a disk is to execute all subtests in the default order.

> **NOTE**
>
> Some individual functions performed during formatting are contained in two separate subtests in order to assist in special testing of drives. Therefore, Subtest 101, Format and Pattern Test should not be invoked unless Subtest 102, Initialize Diagnostic Cylinder is also invoked.

If only Subtest 101, Format and Pattern Test is invoked, the option to quit or continue is available. The test displays the warning message shown in the following figure if only Subtest 101 is invoked:

Figure dev4110–9, System Format and Verification Warning Screen

```
WARNING! SMD Disk Formatter, dev4110, should never be invoked with
         Subtest 101 selected and no Subtest 102.
Do you want to continue [yn]     - y (RETURN)


                                WARNING!!

        YOU HAVE CHOSEN TO ONLY PARTIALLY FORMAT A DRIVE!
        THE DRIVE WILL NOT BE ACCEPTABLE FOR SYSTEM USE!
```

The Class 1 subtests are shown in the following table:

Table dev4110–6, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (hr:min:sec)
100	Input Defects Before Formatting	N/A
101	System Format of SMD	2:20:00[2]
102	Initialize Diagnostic Cylinder	3:00[1]
103	Verify System Format of SMD	5:30[2]
104	Test Diagnostic Cylinder	:15[1]

[1] This test is run sequentially on each drive so multiply this time by the number of drives for an estimate of the required time for this subtest.

[2] Times will double, triple, or quadruple for 2, 3 or 4 drives, respectively, per controller.

Subtest 100, Input Defects Before Formatting

Subtest 100 is used to enter defect map information before pattern testing. The inputs can be entered or can be read from a specified file. In either case, the inputs can be in Byte-Count-After-Index (BCAI) format or in logical sector number format.

A command processor is invoked when this subtest begins. Several commands are available for the input of defects. Startup of this subtest is shown in the following figure:

Figure dev4110–10, Subtest 100 Startup Screen

```
Type 'h' for help with commands
        Logical sector input mode selected.

If you do not have defects to enter, just enter 'q'

make_bad (D1;Sector)->
```

Enter **h** to display a help facility which lists the available commands. The help output is displayed as shown in the following figure:

Figure dev4110–11, Subtest 100 Help Screen

```
Commands:
c[hange_mode]        - toggles logical sector/defect map entry mode
cyl hd sec           - logical sector to be slipped
cyl hd bcai len      - defect map entry to be slipped
del[ete] cyl hd sec - delete logical sector entry
del[ete] cyl hd bcai len - delete defect map entry
dr[ive] [n]          - change/display current drive
f[ile] filename      - get inputs from specified file
h[elp]               - display this information
l[ist]               - list inputs made so far
q[uit]               - exit
!UNIX-command        - execute UNIX command
'comment             - comment; ignored
```

When manually entering defects, first select the entry mode. The default mode is logical sector mode. To enter manufacturer's defects (which are in BCAI format), switch modes with the **change_mode** command. Then enter the position of each flaw. In sector mode, enter the cylinder, head, and sector where the flaw exists. In BCAI mode, enter the cylinder, head, byte-count-after-index, and bit-length.

To enter the defect data from one or more files, select each file by typing

file *filename*

where *filename* is replaced with the actual name of the file. The first line of the file defines the drive type and looks like the following:

n *drivename*

where *drivename* is the drivename which can be found in the file */mnt/bin/lib/DB_diskfmt* on the Service Processor (for example, DKD-005 for the 1/2 GByte NEC 2352 drive). Following the drive name line, the file has remaining lines that contain either BCAI inputs or logical sector inputs. A BCAI input is preceded with the letter **d** while a logical sector input is preceded with the letter **s**. A spare sector can be specified by using a logical sector number one greater than the last used sector number. To specify a track that is to be mapped to an alternate track, use the letter **m** followed by the cylinder and head of the bad track. One or more spaces separate each item in the file and a new line can be started between any two items. Comments may be included in the file by typing a # at any place on a line. All characters from the # to the end of the line are ignored. Blank lines are also allowed. A file containing defect data is shown in the following figure:

Figure dev4110–12, Creating a Defect Data File

```
#------------------------------ start of file ----------------------------
# serial number: 003013
n  DKD-005  # NEC 2352 drive
#   cyl  hd   bcai  len       cyl  hd   bcai  len
d   157  15  24395   34    d  297  14  14102    4  # BCAI Inputs
d   466   0    206    1

#   cyl  hd  sec             cyl  hd  sec
s   457  12   42          s  821   5   11         # Logical sector inputs
#------------------------------ end of file ------------------------------
```

NOTE

To abort *dev4110* while in this subtest, press CTRL and **b**. The SPU takes about 30 seconds to dump memory. Then the SPU prompt is displayed. If CTRL and **c** are pressed, it is intercepted by the subtest and the subtest prompt is displayed.

The current input mode (logical sector or defect map mode) is revealed in the slip prompt. If in logical sector input mode, the prompt appears as follows:

```
make_bad (D1;Sector)->
```

If in defect map input mode, the prompt appears as follows:

```
make_bad (D1;Defect)->
```

When a defect is entered, a list of logical sectors that correspond to the defect is generated as follows:

Figure dev4110–13, List of Logical Sectors For a Defect

```
make_bad (D1;Defect)-> 293 1 572 9510
        Associated logical sectors: 59 0 1
```

The previous figure illustrates that three sectors are affected by the media flaw which starts at byte 572 from index and is 9510 bits long.

The byte before and after any flaw is also considered bad to avoid the possibility that a flaw might be slightly bigger than is reported in the defect map.

If two defects affect the same sector, the logical sector is only entered in the *INPUTS THAT WILL BE SLIPPED* input list once. Subsequent entries of the same sector are entered in the *INPUTS THAT WILL NOT BE SLIPPED* list.

For instance, if the following two defects exist:

cylinder	head	bcai	bit-length
10	0	70	1
10	0	80	1

Both defects fall in sector 0 so when the second defect is entered, it does not create a new entry in the input list. This is shown in the following figure:

Figure dev4110–14, Two Defects Entered for the Same Sector

```
make_bad (D1;Defect)-> 10 0 70 1
     Associated logical sectors: 0
make_bad (D1;Defect)-> 10 0 80 1
     Associated logical sectors: (0)
```

The following is an example of entering a bad location and deleting it:

Figure dev4110–15, Entering and Correcting An Incorrect Location

```
make_bad (D1;Sector)-> 17 7 23
make_bad (D1;Sector)-> 17 7 46
make_bad (D1;Sector)-> d 17 7 46
        Input 17 7 46 has been removed
make_bad (D1;Sector)-> list

 INPUTS THAT WILL NOT BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
         ---------------------- no sectors ----------------------

 INPUTS THAT WILL BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
 17  7  23
```

The following is an example of switching drives and entering defects for the drive from a file:

Figure dev4110–16, Entering Defects for a New Disk Drive

```
make_bad (D1;Sector)-> dr 2
        Drive 2 is now selected
make_bad (D2;Sector)-> !cat SN12345678          <-to illustrate unix cmd
# Serial Number: 12345678
d  100  5 10536     1
d  257  9 26401  1000
> file SN12345678                                <-prompt after unix cmd is '>'
make_bad (D2;Sector)-> list

 INPUTS THAT WILL NOT BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
         ---------------------- no sectors ----------------------

 INPUTS THAT WILL BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
 100  5  11  10536     1      N/A USR | 257  9  35  26401  1000      N/A USR
 257  9  36  26401  1000      N/A USR |

make_bad (D2;Sector)->
```

In the above example, the manual mode is set to `Sector` but the file contains BCAI information. This is does not create a problem. The manual mode only applies to manual inputs. File inputs are controlled by the character that precedes the defect location. The defect at cylinder 257, head 9 was large enough to overlap two sectors so both were flagged bad.

Type **quit** after entering all inputs to exit the subtest. Then Subtest 101 starts.

Subtest 101, System Format of SMD

Subtest 101 formats a drive for system use except for the creation of the diagnostic cylinder which is performed in Subtest 102, Initialize Diagnostic Cylinder. This subtest consists of the following five parts:

1. Format with no spare sectors to allow pattern test of all sectors.
2. Pattern test by first reading the `0x00000000` pattern which was written during format. Then write and read seven other patterns which are shown below:

   `0xAAAAAAAA` `0xAF5BAF5B`
   `0xFFFFFFFF` `0x5EB75EB7`
   `0xEBD6EBD6` `0x6DB66DB6`
   `0xD7ADD7AD`

   These patterns can be replaced by up to 16 other patterns if the file *dev4110.patt* is created in the current directory or if it is created in */mnt/bin/lib*. The current directory is searched first. The format of the file is free form with eight hex characters per pattern and at least one space separating the patterns. More than one line can be used to define the patterns. Blank lines are also allowed.

Any sector-related errors (header not found; hard ECC error; or correctable ECC error) are retried immediately and, if an error occurs again in ten retries (does not have to be the same error), the sector location is saved for later slipping. A maximum of 1365 errors can be saved per drive. The maximum includes the flaws from Subtest 100, Input Defects Before Formatting. Errors that do not repeat are discarded. If a verbose value of 2 is selected, each error is printed at the time it is detected.

3. Format with one spare sector per track.
4. Slip sectors which were input in Subtest 100, Input Defects Before Formatting or which were detected as bad during pattern test. If more than one sector is bad on a track, one sector is slipped and then the remaining bad sectors are added to the bad block table. This table associates the bad sectors with good sectors located in the last and possibly next to the last cylinder. Up to 639 sectors can be relocated.

   If a verbose value of 1 (default) is selected in the test parameter menu, a summary of bad sectors for each drive is printed before slipping occurs.
5. The last operation is to write five copies of the bad block table to the last 25 sectors of the disk.

Subtest 102, Initialize Diagnostic Cylinder

Subtest 102 writes special patterns to the diagnostic cylinder which is the cylinder just before the cylinder used for relocated sectors. Sector 0 of each track contains a table of contents that describes what is written to each of the remaining sectors. If no sectors have been relocated on a track, sector 1 is marked bad. The next twelve sectors contain Error Correction Code (ECC) errors of length 1 to 12 respectively. The remaining sectors have the seven patterns listed in Subtest 101, System Format of SMD written to them. Sector 13 (or 14 if sector 1 is marked bad) will contain an `0xAAAAAAAA` pattern, sector 14 (or 15) will contain an `0xFFFFFFFF` pattern, and so on with the patterns repeating every seven sectors. Refer to the section Disk Parameters File, *DB_diskfmt* Description for more information about the diagnostic cylinder.

Subtest 103, Verify System Format of SMD

Subtest 103 reads every logical sector in the usable portion of the disk. The usable portion of each drive is all the cylinders preceding the diagnostic cylinder and all relocated sectors (which are found on the innermost one or two cylinders). When a header not found error occurs, the bad block table is checked to see if the header has been relocated. If it has been relocated, the alternate sector is read.

Any errors other than those due to sector relocation are reported and count against the device errors per subtest limit. If the number of errors exceeds the limit, the drive is failed.

Subtest 104, Test Diagnostic Cylinder

Subtest 104 reads each sector on the diagnostic cylinder and expects soft or hard ECC errors on sectors 1 through 12 of each track (or sectors 2 through 13 if sector 1 is marked bad). The remaining sectors must be error-free.

Class 2 Subtest

The Class 2 subtest performs interactive testing of all selected drives. The Class 2 subtest can only be started by explicitly using the **-c** or **-s** options when *dev4110* is invoked. The Class 2 subtest is shown in the following table.

Table dev4110–7, Class 2 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
200	Interactive Test	N/A

Subtest 200, Interactive Test

Subtest 200 provides a special interactive test interface to perform the following disk maintenance tasks:

- Pattern test portions of the disk
- Slip bad sectors
- Format single tracks
- Several more useful operations

A help facility is available when needed.

> **CAUTION**
>
> Three of the interactive test commands are potentially data destructive: **format**, **pattern_test**, and **slip_sectors**.

Each command performs an automatic save of the data it is to overwrite before the operation begins. However, the commands can still be data destructive if one of the following actions is attempted:

1. An attempt to pattern test more than one track is performed and **y** is entered when asked to confirm multiple track pattern test (because only one track can be saved).
2. An attempt to preserve a track's data before a destructive operation fails and a response is entered to force the operation anyway.
3. The pattern test, slip sectors, or format operation has completed and then data errors occur during the restore of the track's data.
4. The keys CTRL and **c** or CTRL **b** are pressed in the middle of the operation.
5. Automatic save is disabled by using the **toggle_save** command.
6. A power outage or some other unforeseen event causes the test to abort in the middle of the operation.

Interactive Test Invocation

To invoke the interactive test, use the procedure shown in the following figure:

Figure dev4110–17, Interactive Test Invocation Sequence

```
(spu)> cd /mnt/test
(spu)> mminit -s
(spu)> dshell
: test dev4110 -c 2 (or test dev4110 -s 200)
```

Interactive Test Parameter Menu

The prompts are displayed as shown in the following figure. Use defaults for the first four prompts and then select the drives to test and press RETURN after each drive is selected. After all drives have been selected, press RETURN twice and enter **y**. After about a minute, the interactive test will start.

The following figure shows the prompts for the Interactive Test Parameter Menu:

Figure dev4110–18, Interactive Test Parameter Menu

```
                        ENTER TEST PARAMETERS
          []      Encloses allowed input ranges or values
          ()      Encloses the default value
          ^       Returns to the previous prompt
          :nn     Returns to the prompt # nn
          :       Returns to the first unsatisfied prompt

          ?       Prints an additional help menu
 1:  Number of errors allowed per device each subtest
    [0-65535]                                          (0) -> RETURN
 2:  Number of devices failed before test aborts
    [0-65535]                                         (12) -> RETURN
 3:  Verbosity of test [0-65535]                       (3) -> RETURN
 4:  Ioconfig file                              (/ioconfig) -> RETURN
                PERIPHERAL CONFIGURATION DATA[1]
     IOP  MBUS  TYPE       CSR    INT  UNIT  TYPE
     ---  ----  --------  -----   ---  ----  -------
 1)   3     0   DKC-001   0xdc0    1     0   DKD-001
 2)   3     0   DKC-001   0xdc8    4     0   DKD-001
 3)   6     1   DKC-001   0x3f0    3     0   DKD-001
Enter device 99 to begin user-defined configurations or 0 to end selection

 5:  Device selection [0,1-3,99]                       (0) -> 1 RETURN
 6:  Device selection [0,1-3,99]                       (0) -> 2 RETURN
 7:  Device selection [0,1-3,99]                       (0) -> 3 RETURN
 8:  Device selection [0,1-3,99]                       (0) -> RETURN
 9:  Enter OK, or :NN to return to question NN [OK]
                                                      (OK) -> RETURN

   ********** WARNING! **********
THIS TEST IS POTENTIALLY DISK DATA DESTRUCTIVE!
IF YOU CONTINUE, DATA COULD BE LOST!
Do you want to continue [yn]      -> y RETURN
```

[1] This information is only displayed once; to display it again , type **i** RETURN at any prompt during test parameter query.

Interactive Test Mode

After the test parameter menu prompts have been answered the following is displayed indicating interactive test mode:

> **NOTE**
>
> In the following figure, D1 indicates drive 1 is selected and Save indicates that track data is saved during the data destructive commands **format**, **pattern_test**, and **slip_sectors**.

Figure dev4110–19, Interactive Test Mode

```
                    INTERACTIVE TEST MODE
                       FOR SMD DRIVES

Type 'h' for help
(D1;Save)->
```

Type **h** to list the available interactive test commands. For additional help, refer to the command descriptions in the following section. Only a unique portion of the beginning of a command needs to be typed.

To exit the interactive test, type **q** and press RETURN. If a track is saved, a prompt is displayed indicating whether data can be lost. If **y** is entered or if a track is not saved, *dev4110* ends normally and exits back to the dshell prompt. If **n** is entered, the test returns to the interactive prompt without executing changes.

Interactive Test Commands

The following table lists the available commands and also a description of each command.

Table dev4110–8, Interactive Test Commands

COMMAND	DESCRIPTION
a[lternate_seek]	Seek between two selected cylinders
b[bt_display]	Display Bad Block Table
d[rive_select]	Select a drive
f[ormat]	Reformat one track
hd[e_display]	Display header, data, and ECC
h[elp]	Display list of commands and their arguments
i[nitialize_bbt]	Rebuild damaged Bad Block Table
p[attern_test]	Pattern test range of sectors
q[uit]	Exit from the Interactive Test
r[estore_track_data]	Restore previously saved track data
sa[ve_track_data]	Save one track's data
sc[an_flaws]	Produce file of all marked-bad sectors
se[ctor_display]	Display data from range of sectors
sl[ip_sectors]	Slip one or more sectors
st[atus]	Display current drive and which track is saved
to[ggle_save]	Switches between allowing and disabling auto-save
tr[ack_headers_display]	Display track headers
v[erify_format]	Read a range of sectors
!UNIX-command	Execute UNIX command
'comment	Any comment; ignored

Interactive Test Commands Descriptions

The following sections describe the interactive test commands.

Seek Between Two Selected Cylinders

a[lternate_seek]

This command performs seeks between two selected cylinders.

Display Bad Block Table

b[bt_display]

This command displays the active drive's bad block table as follows:

Figure dev4110–20, Active Drive's Bad Block Table Display Screen

```
BAD BLOCK TABLE FOR ccu/mb/csr/d=3/0/3f0/0

         CYL HD SEC  CYL HD SEC  CYL HD SEC  CYL HD SEC  CYL HD SEC
         275  3  48  387 11  48
```

When one bad sector is slipped on a track, the bad sector is slipped and all subsequent sector headers are shifted by one with the last logical sector replacing the spare sector. Additional slipped sectors on a track causes the associated headers to be marked bad and the sectors to be relocated. To display which sectors are bad, use the **track_headers_display** command. The bad sectors are flagged with a *B. To display a different drive's bad block table, use the **drive_select** command to change drives.

Select a Drive

d[rive_select] [*drive-number*]

This command can change which drive is the active drive. Most of the other commands operate on the active drive only. The argument ***drive-number*** is the entry number from the Drive Configuration Data which was displayed at the end of the user prompts. To display the entry numbers, enter **d** and press RETURN. The Drive Configuration Data and active drive are then redisplayed, and a prompt is displayed to enter a new drive entry number. Enter **0** or press RETURN for the current drive.

Use of the **drive_select** command is shown in the following figure:

Figure dev4110–21, Drive Configuration Data Screen

```
(D1;save)-> d

                    DRIVE CONFIGURATION DATA

    IOP MBus MBus  Int   Unit  #    #  Phys  Log
     #   #   CSR  Level   #   Cyl  Hds  Sec  Sec  Name
    --- --- ----- -----  ---  ---  ---  ---  ---  -------
 1.  3   0  0x3f0   2     0   760   19   60   59  DKD-005
 2.  3   0  0x3f0   2     1   760   19   60   59  DKD-005
 3.  3   0  0x3f8   3     0   842   20   46   45  DKD-001

       Drive 1 is currently selected
       Enter new selection or 0 to leave it as is (0,1-3) [0] -> 2
       Drive 2 is now selected
(D2;save)-> d 3
       Drive 3 is now selected
(D3;save)->
```

The configuration data does not display if the drive number is entered. Also, the drive number is redisplayed with each prompt as D*x* where *x* is the current drive number.

Reformat One Track

f[ormat] *cyl hd*

This command unslips sectors or recreates a bad track's headers. If automatic save is enabled (the prompt indicates Save), then before the track is reformatted, an attempt is made to read every logical sector (including relocated sectors). If a read fails, the options of retrying the sector, terminating the format before any destructive operation occurs, or forcing the format even though one or more sectors may not be recovered are displayed.

> **CAUTION**
>
> If auto save is disabled (Nosave mode) by using the **toggle_save** command, the track is reformatted without preserving the track's data.

In the following figure, cylinder 300, head 12 is reformatted on an NEC drive (760 cylinders, 19 heads, 59 logical sectors). The track contains two slipped sectors as shown. The second bad sector has been relocated.

CAUTION

If auto save is enabled and sectors are unslipped by the **format** command, data is restored to the bad sectors which could cause the data to no longer be readable. This is okay since the data is still saved. Slip the bad sectors using the **slip_sectors** command and then use the **restore_track_data** command to restore the track's data.

The following figure shows how to perform the restoration operation:

Figure dev4110–22, Formatting a Track

```
(D3;Save)-> format 300 12
        No data has been previously saved. Saving this track
        Data save operation complete

  TRACK HEADERS BEFORE FORMAT:
 cylinder = 300  head = 12
 47 48 49 50 51 52 53 54 55 56 57 58  0  1  2  3 *B  4  5  6  7  8  9 10 11
 12 13 14 *B 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
 37 38 39 40 41 42 43 44 45 46

        About to format cylinder 300  head 12. Are you sure? [yn] -> y
        Format complete.  2 sectors have been unslipped.
        Restoring data to track
        Data restore operation complete
(D3;Save)-> track 300 12
 cylinder = 300  head = 12
 48 49 50 51 52 53 54 55 56 57 58 *S  0  1  2  3  4  5  6  7  8  9 10 11 12
 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
 38 39 40 41 42 43 44 45 46 47
(D3;Save)->
```

Then pattern test the track and identify which sectors are bad, and slip the bad sectors. Then restore the original track data. These operations are shown in the following figure:

Figure dev4110–23, Restoring the Original Track Data

```
(D3;Save)-> patt 10 times 300 12 0 to 300 12 58
     Patterns used:
      aaaaaaaa ffffffff ebd6ebd6 d7add7ad af5baf5b 5eb75eb7 6db66db6
        If you save this track, you will lose the saved data for
        drive 3: cylinder 300  head 12.
        Save data? [yn] -> n                <- previous data is what you want
        WARNING - DATA NOT SAVED

 pass # 1
dev4110 ERROR (0x1e) ccu/mb/csr/d 3/0/3f0/0 - Correctable ECC error
 cyl: 300 hd: 12 sec: 4

dev4110 ERROR (0x06) ccu/mb/csr/d 3/0/3f0/0 - Hard ECC error
 cyl: 300 hd: 12 sec: 16

---- more errors will be detected as the test loops. ----

(D3;Save)-> slip
slip (D3;Save;Sector)-> 300 12 4
slip (D3;Save;Sector)-> 300 12 16
slip (D3;Save;Sector)-> e

 INPUTS THAT WILL NOT BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
         ---------------------- no sectors ----------------------

 INPUTS THAT WILL BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
 300 12   4                  N/A USR | 300 12  16                  N/A USR

        Are you sure inputs are ready for slipping? [yn] -> y
      sector 300 12  4 and
             300 12 16: slipped
(D3;Save)-> restore
        Data has been saved for drive 3: cylinder 300 head 12
        Do you really want to restore this data? [yn] -> y
        Data restore operation complete
(D3;Save)->
```

Display Header, Data, and ECC

hd[e_display] *cyl hd sec* [**to** *cyl hd sec*]

This command is used to display the sector data, the header, and ECC. The data is read in raw mode; therefore, the controller does not perform error checking.

> **NOTE**
>
> The sector specified for the **hde_display** command is the physical sector numbered from index. All other commands search all headers on the track until the requested header is found.

To illustrate the **hde_display** command, the track headers displayed by the **track** command and the sector displayed by the **hde_display** command are shown in the following figure:

Figure dev4110–24, *hde_display* Command

```
(D2;Save)-> track 27 5
 cylinder =  27  head =  5
 55 56 57 58 *S  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19
 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44
 45 46 47 48 49 50 51 52 53 54
(D2;Save)-> hde 27 5 0

Phys:  27  5   0  Log:  27  5  55  Type: 0        Header:001b0537 ECC:2bc18e26
000  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
020  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
040  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
060  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
080  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0a0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0c0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0e0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
100  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
120  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
140  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
160  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
180  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1a0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1c0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1e0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6

(D2;Save)->
```

The previous figure shows that the physical sector 0 corresponds to logical sector 55 on this track.

Display List of Commands and Arguments

h[elp]

This command lists the commands and their arguments.

Rebuild Damaged Bad Block Table

i[nitialize_bbt]

This command reads the Bad Block Table (BBT) and attempts the following:

1. Tries to read (successfully)any one of the five copies in the BBT
2. If any one of the copies is read successfully, it is used to recreate all of the other copies
3. If none of the copies in the BBT are read successfully, a message is printed out stating that all copies of the BBT are bad. The following prompt is then printed:

```
Do you want to retry the last operation [yn] ->
```

If this prompt is answered with **y**, program will attempt to read (successfully) the BBT again. If **n** if entered, the following prompt will be displayed:

```
WARNING:  This could result in several NEW Header Not Found Errors.

Do you want to continue [yn] ->
```

> **WARNING**
>
> If the previous prompt is answered with **y**, any previous entries to the BBT will be erased. Run *verify_format* and take appropriate action if any Header Not Found messages appear.

The following figure displays an example of this command:

Figure dev4110–25, Initialize_bbt Example

```
(D1;Save)-> initialize_bbt
Drive 1: BBT copy 1 is bad.  Count field is 2779096485. Should be 0-638.
Drive 1: BBT copy 2 is bad.  Count field is 2779096485. Should be 0-638.
Drive 1: BBT copy 3 is bad.  Count field is 2779096485. Should be 0-638.
Drive 1: BBT copy 4 is bad.  Count field is 2779096485. Should be 0-638.
Drive 1: BBT copy 5 is bad.  Count field is 2779096485. Should be 0-638.


dev4110 ERROR (0x4d)-ccu/mb/csr/d=7/3f0/0 All copies of BBT are bad
The internal copy of the BBT is cleared since no good copies were found
Do you want to retry the last operation [yn] -> y
Drive 1: BBT copy 1 is bad.  Count field is 2779096485. Should be 0-638.
Drive 1: BBT copy 2 is bad.  Count field is 2779096485. Should be 0-638.
Drive 1: BBT copy 3 is bad.  Count field is 2779096485. Should be 0-638.
Drive 1: BBT copy 4 is bad.  Count field is 2779096485. Should be 0-638.
Drive 1: BBT copy 5 is bad.  Count field is 2779096485. Should be 0-638.


dev4110 ERROR (0x4d)-ccu/mb/csr/d=7/3f0/0 All copies of BBT are bad
The internal copy of the BBT is cleared since no good copies were found
Do you want to retry the last operation [yn] -> n

WARNING: This could result in several NEW Header Not Found Errors.

Do you want to continue [yn] -> y
Done
```

Pattern Test a Range of Sectors

p[attern test] [*nnn* **times**] *cyl hd sec* [**to** *cyl hd sec*] [**with** *pat1* [*pat2...*]]

This command pattern tests the selected sectors repetitively. It is used to test part or all of the system portion of the disk (all cylinders before the diagnostic cylinder and relocated sectors). If the test is constrained to one track, the data is automatically saved and restored when the operation is completed. If more than one track is selected, a warning prompt is displayed and the operation can be terminated at that point to prevent permanent overwrite of data. The automatic save can be disabled with the **toggle_save** command. The argument [**to** *cyl hd sec*] can be substituted with the argument [**to** *end*].

Arguments:

- [*nnn* **times**]— Repetition count. possible responses include:
  - **1**—Lower bound value, default value.
  - **2,147,483,647**—Upper bound value.
- *cyl hd sec*— Starting sector.
- [**to** *cyl hd sec*] Ending sector, default is starting sector.
- [**with** *pat1*[*pat2...*]]— Up to 16 4-byte hex patterns can be specified. The default is the following seven patterns: `aaaaaaaa ffffffff ebd6ebd6 d7add7ad af5baf5b 5eb75eb7 6db66db6`

Restore Previously Saved Track Data

r[estore_track_data]

This command can restore data from the general buffer to the original track (the track where the data was originally stored). The **save_track_data** command stores data from a selected track into the general buffer. In addition, the **format** and **pattern_test** commands save into the general buffer before their operation and automatically restore the data afterward. The data remains in the buffer so it can be restored again at a later time if, for instance, the first restore was bad.

If data is saved and not restored and then an attempt is made to quit the interactive test, a message is displayed indicating there is saved data and a prompt is displayed that allows reentering the interactive test or exiting the test.

The following figure shows an example of using the restore command:

Figure dev4110–26, Restore Command Example

```
(D3;Save)-> restore
        Data has been saved for drive 3: cylinder 273  head 17
        Do you really want to restore this data? [yn] -> y
        Data restore operation complete
(D3;Save)->
```

If **n** is entered, the data is not restored, the operation is terminated, and the test returns to the interactive test prompt.

If the current drive has been changed from drive 3 to drive 9 since the last save operation, the following is displayed:

Figure dev4110–27, Changing Drives Since Last Save Operation

```
(D9;Save)-> restore
        Data has been saved for drive 3: cylinder 273  head 17
        However, drive 9 is currently selected.
        Use 'd[rive_select]' to change drives and try again.
(D9;Save)->
```

If data was not saved before attempting to restore the data, the following is displayed:

Figure dev4110–28, Attempting to Restore Data Before Saving

```
        No data has been previously saved so restore aborted.
(D9;Save)->
```

Save One Track of Data

sa[ve_track_data] *cyl hd*

This command saves one track of data into the general buffer. The data can be restored with the **restore_track_data** command. Data on relocated sectors is also saved so, if the track is reformatted (which removes the relocated sectors), all the track's data can be restored.

> **NOTE**
>
> The prompt in the following figure specifies **Nosave**. This indicates the command **toggle_save** has previously been entered so saves are not automatic on destructive operations. It has no affect on this command. Normally, **Save** appears since disabling automatic save can be data destructive.

The following is an example of saving one track:

Figure dev4110–29, Saving One Track

```
(D4;Nosave)-> save 525 5
        Data has already been saved for drive 4: cyl=601, hd=14
        Are you sure you want to overwrite this data? [yn] -> y
        Data save operation complete
(D4;Nosave)->
```

Produce File of All Bad Sectors

sc[an_flaws] *filename*

This command reads every header on the disk looking for headers marked bad or which contain invalid information. Each of these headers produces an entry in the ASCII file entered on the command line. The file is in the same format as is read by the **file** command in Subtest 100, Input Defects Before Formatting. Refer to Subtest 100 for a description of the file format.

Display Data From Range of Sectors

se[**ctor_display**] *cyl hd sec* [**to** *cyl hd sec*]

This command displays the data from one or more consecutive sectors.

The following figure shows an example of the **sector_display** command:

Figure dev4110–30, Displaying Sector Data

```
(D1;Save)-> sector 27 5 55

        Sector  27  5 55:
000  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
020  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
040  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
060  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
080  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0a0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0c0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0e0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
100  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
120  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
140  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
160  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
180  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1a0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1c0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1e0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6

(D1;Save)->
```

This example is almost identical to the example for the **hde_display** command. The major difference in the two methods is that with the **sector_display** command, the read is sensitive to data errors. In the raw read mode that the **hde_display** command uses, no data errors are reported. If a data error does occur while executing the **sector_display** command, it is retried 10 times and any successful read results in the sector being displayed without an error message. If ten unsuccessful attempts to read the sector occur, then an error message is displayed and a prompt is displayed whether to retry, force, or skip the read.

To retry the read another 10 times press (RETURN). To retry the read a different number of times, enter a number. From 1 to 2,147,483,647 retries can be specified. Every five retries a seek is alternately performed one cylinder in and back or one cylinder out and back.

If **force** is entered for the read, the buffer the data was supposed to be read into is displayed. If an ECC error occurred, the data is whatever was read. If some other error occurred, the data may be whatever was in the buffer before the read and be invalid. The error reported is the last error that occurred; it can be used to determine if the data is valid.

> **NOTE**
>
> At present, the software does not correct the data if it is a correctable ECC error.

If **skip** is entered, the sector is skipped. If there are more sectors to read in the range specified, then the display continues with the next sector.

The following is an example of a read that fails:

Figure dev4110–31, Failed Read Example

```
(D1;Save)-> sector 400 22 18 to 400 22 19

dev4110 ERROR (0x06) ccu/mb/csr/d 3/0/3f0/1 - Hard ECC Error
 cyl:400 hd:22 sec:18

                        10 attempts to read sector failed
                        what to do [# of retries/force/skip] (10) -> 100

dev4110 ERROR (0x06) ccu/mb/csr/d 3/0/3f0/1 - Hard ECC Error
 cyl:400 hd:22 sec:18

                        100 attempts to read sector failed
                        what to do [# of retries/force/skip] (100) -> skip

        Sector 400 22 19
000  00000000 00000000 00000000 ff300020  1023eee10 99903220 b2d3d4d1 ab222290
020                     ------------ and so on -------------
```

Sector 18 was not displayed since it was skipped. What was displayed was the next sector, sector 19 which was read successful. The next sector (sector 19) was displayed because it was read successfully in one of the first 10 attempts.

Slip One or More Sectors

sl[ip_sectors]

CAUTION

Read the caution and following example at the end of this command's description before using this command.

This command is used to slip sectors which are generating errors or to enter defect map information to **slip sectors**. If automatic save of track data is enabled (indicated by Save in the prompt), an attempt to save and restore all sectors is made to minimize data loss unless automatic save is disabled with the **toggle_save** command.

Entering the **slip_sectors** command starts a separate command processor which expects bad sectors or defect map information to be entered. A help facility which lists the available commands is displayed if **h** is entered. The help output appears as follows:

Figure dev4110–32, *slip_sectors* Command Help Screen

```
SLIP_SECTORS commands:
c[hange_mode]          - toggles logical sector/defect map entry mode
cyl hd sec             - logical sector to be slipped
cyl hd bcai len        - defect map entry to be slipped
d[elete] cyl hd sec    - delete logical sector entry
d[elete] cyl hd bcai len - delete defect map entry
e[xecute]              - slip the sectors now
h[elp]                 - display this information
l[ist]                 - list inputs made so far
q[uit]                 - exit from 'slip_sectors'
!unix-command          - execute unix command
'comment               - comment; ignored
```

To slip sectors which are generating errors, the normal usage is to display the track headers for each track on which a sector is to be slipped by using the **track_headers_display** command. This command displays the headers before they are altered so the slip can be verified. Then enter all sectors which need to be slipped, verify the entries using the **list** command, delete any incorrect entries with the **delete** command, and then begin the slip with the **execute** command. New sectors can be entered at any time until the **execute** command is completed. As a safeguard, when the **execute** command is entered, the list of sectors is automatically displayed and a prompt is displayed to confirm the list. If **n** is entered, execution returns to the **slip_sectors** prompt with all inputs still intact.

To exit the test at any time enter the **quit** command.

To enter defect map information, first enter the **change_mode** command and then follow the above procedure. It may not be desirable to display track headers if there is a large number of tracks.

NOTE

When entering the defect map for a new disk, a disk that has just been formatted and does not yet contain a file system, the automatic save may be disabled with the **toggle_save** command before entering the **slip_sectors** command. This causes the slip to proceed much faster.

CAUTION

If the **toggle_save** command is executed prior to the slip, any usable data that exists on the disk will be lost, so use this approach with caution.

The current input mode (logical sector or defect map mode) is revealed in the slip prompt. If logical sector input mode is selected, the prompt appears as follows:

```
slip (D1;Save;Sector)->
```

If defect map input mode is selected, the prompt appears as follows:

```
slip (D1;Save;Defect)->
```

When a defect is entered, the associated track's headers are immediately read and a list of logical sectors that correspond to the defect are listed as shown in the following figure:

Figure dev4110–33, Entering a Defect

```
slip (D1;Save;Defect)-> 293 1 572 9510
        Associated logical sectors: *S 0 1
```

The previous figure illustrates that three sectors are affected by the media flaw which starts at byte 572 from index and is 9510 bits long. The *S indicates that one of the affected sectors is the spare sector. If a *B is displayed, then the media defect affects an already bad sector which is not reslipped.

The byte before and after any flaw is also considered bad to avoid the possibility that a flaw might be slightly larger than is reported in the defect map.

If two defects affect the same sector, the logical sector is only entered in the *INPUTS THAT WILL BE SLIPPED* input list once. Subsequent entries of the same sector are entered in the *INPUTS THAT WILL NOT BE SLIPPED* list. For example, the following two defects exist:

cylinder	head	bcai	bit-length
10	0	70	1
10	0	80	1

Both defects are in sector 0 so when the second defect is entered, the sector is not slipped again. The slipping of a sector with two defects is shown in the following figure:

Figure dev4110–34, Slipping Sectors With Two Defects

```
slip (D1;Save;Defect)-> 10 0 70 1
        Associated logical sectors: 0
slip (D1;Save;Defect)-> 10 0 80 1
        Associated logical sectors: (0)
        Sectors in () have already been input and will not result in a new
        entry. A (*G) means the flaw falls entirely in a gap and is ignored.
slip (D1;Save;Defect)-> list

 INPUTS THAT WILL NOT BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
  10  0   0     80     1       N/A USR |

 INPUTS THAT WILL BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
  10  0   0     70     1       N/A USR |
```

The above example also refers to a *gap* which is listed in the Associated logical sectors list as a (*G). The *G indicates that the entire media flaw was in a space between sectors or located after the last sector on the track.

NOTE

In the current version of the *dev4110* test, no bytes are considered part of a gap. A flaw in any byte results in one or more sectors being slipped.

When the slip is executed, the sectors are slipped one track at a time. If automatic save is active, the data for the track is copied to a special buffer (not the general buffer used by the **save_track_data** command) before the slip and is restored after the slip. One problem exists which is that correctable ECC errors are not corrected so a correctable ECC error may not be fixable without a loss of data.

To verify the slip, display the track headers once more. All slipped sectors are marked with a ***B**.

An example of slipping the sectors 17 7 23, 17 7 36, 247 12 4, and 255 0 12 is shown in the following figure:

NOTE

Track 255 already has a slipped sector. Sector 12 that is about to be slipped *must* be a new error since sector 6 was slipped. Refer to the caution and following example at the end of the **slip_sectors** command description for more information about slipping two or more sectors on one track.

Figure dev4110–35, Display Slipped Track Headers

```
(D1;Save)-> track 17 7
cylinder =  17  head =  7
53 54 55 56 57 58 *S  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17
18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42
43 44 45 46 47 48 49 50 51 52
(D1;Save)-> track 247 12
cylinder = 247  head = 12
48 49 50 51 52 53 54 55 56 57 58 *S  0  1  2  3  4  5  6  7  8  9 10 11 12
13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
38 39 40 41 42 43 44 45 46 47
(D1;Save)-> track 255 0
cylinder = 255  head =  0
 0  1  2  3  4  5 *B  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48
49 50 51 52 53 54 55 56 57 58
```

If defect input mode is selected and an attempt is made to slip the sector on track 255 head 0 which has already been marked bad in the previous figure, the following figure shows what would be displayed:

Figure dev4110–36, Slipped Tracks Previously Marked Bad

```
slip (D1;Save;Defect)-> 255 0 3800 1
        Associated logical sectors: (*B-61)
```

The associated logical sector has been previously marked bad (*B). The 61 indicates the sector's location from index. Starting with the first sector after index as 0, the sector marked bad is sector 6 after index (which is actually the seventh sector after index). This notation is necessary because, once a header is marked bad, the header no longer contains a logical sector number. The only known information is the header's position from index.

The following illustration shows how to delete incorrect **slip_sectors** inputs:

Figure dev4110–37, Deleting Incorrect *slip_sectors* Inputs

```
(D1;Save)-> slip
Type 'h' for help with slip commands
slip (D1;Save;Sector)-> 17 7 23
slip (D1;Save;Sector)-> 17 7 46
slip (D1;Save;Sector)-> d 17 7 46
        Sector  17  7 46 has been removed from the inputs
slip (D1;Save;Sector)-> list

 INPUTS THAT WILL NOT BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
         ---------------------- no sectors ----------------------

 INPUTS THAT WILL BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
  17  7  23                   N/A USR |


slip (D1;Save;Sector)-> 17 7 36
slip (D1;Save;Sector)-> 247 12 4
slip (D1;Save;Sector)-> 255 0 12
slip (D1;Save;Sector)-> e

 INPUTS THAT WILL NOT BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
         ---------------------- no sectors ----------------------

 INPUTS THAT WILL BE SLIPPED:
 CYL HD SEC   BCAI   LEN LOC  ERR SRC | CYL HD SEC   BCAI   LEN LOC  ERR SRC
  17  7  23                   N/A USR | 247 12   4                   N/A USR
  17  7  36                   N/A USR | 255  0  12                   N/A USR

        Are you sure inputs are ready for slipping? [yn] -> y

      sector  17  7 23 and
              17  7 36: slipped
      sector 247 12  4:
dev4110 ERROR (0x06) ccu/mb/csr/d 3/0/3f0/1 - Hard ECC error
 cyl:247 hd:12 sec:4

                      10 attempts to read sector failed
                      what to do [# of retries/force/skip] (10) -> 100

slipped
        sector 255  0 12: slipped
```

Sector 247 12 4 was difficult to read. After the first 10 attempts failed, a request was entered to retry 100 times. One of the 100 retries was successful so the sector slip operation was completed. If the 100 retries had been unsuccessful, a prompt to retry again, force continuation with the data that had been read from sector 4, or skip slipping this sector would have been displayed. If **skip** is selected, the remaining slips are still performed. Every five

retries a seek is alternately performed one cylinder in and back or one cylinder out and back.

To verify the slips, display the track headers again as shown in the following figure:

Figure dev4110–38, Displaying the Track Headers

```
(D1;Save)-> track 17 7
cylinder =  17  head =  7
52 53 54 55 56 57 58  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17
18 19 20 21 22 *B 23 24 25 26 27 28 29 30 31 32 33 34 *B 36 37 38 39 40 41
42 43 44 45 46 47 48 49 50 51
(D1;Save)-> track 247 12
cylinder = 247  head = 12
47 48 49 50 51 52 53 54 55 56 57 58  0  1  2  3 *B  4  5  6  7  8  9 10 11
12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
37 38 39 40 41 42 43 44 45 46
(D1;Save)-> track 255 0
cylinder = 255  head =  0
 0  1  2  3  4  5 *B  6  7  8  9 10 11 *B 13 14 15 16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48
49 50 51 52 53 54 55 56 57 58
(D1;Save)->
```

Track 17 7 and track 255 0 now have only 58 logical sectors because one sector has been relocated from each track. The Bad Block Table may be displayed as shown in the following figure to verify the relocation actually occurred:

Figure dev4110–39, Displaying the Bad Block Table

```
(D1;Save)-> bbt

BAD BLOCK TABLE FOR ccu/mb/csr/d=3/0/3f0/0

         CYL HD SEC  CYL HD SEC  CYL HD SEC  CYL HD SEC  CYL HD SEC
          17  7  35  255  0  12

(D1;Save)->
```

If there had already been entries in the table, they would have been displayed also. This list of the Bad Block Table is a copy of the table in main memory. However, it does reflect what is on the disk since both the **slip_sectors** and **format** commands rewrite all five copies of the Bad Block Table before returning to the interactive prompt.

Execute the **verify_format** command for each of the tracks to verify the tracks.

CAUTION

The **slip_sectors** command has an inherent danger. If logical sectors are input to be slipped and two or more sectors are to be slipped on the same track, all the sectors that are on the same track must be slipped at one time since the entered sector numbers that are given to **slip_sectors** are logical numbers. **Slip_sectors** searches the headers on the track to find the sectors to slip. If a slip of one sector on a track is executed and then later a slip of another sector is executed (without reverifying the logical sector number of this second sector), the wrong sector might be slipped.

The following is an example to illustrate the preceding caution.

Cylinder 25, head 0 in sectors 8 and 12 is generating correctable ECC errors; therefore, the **track** command is executed as shown in the following figure to display the headers before the slip is performed:

Figure dev4110–40, Display Track Headers Prior to Slipping

```
(D1;Save)-> track 25 0
cylinder =  25  head =  0
 0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49
50 51 52 53 54 55 56 57 58 *S
```

The following figure shows the headers that are displayed if only sector 8 is slipped:

Figure dev4110–41, Display Slipped Track Headers

```
(D1;Save)-> track 25 0
cylinder =  25  head =  0
 0  1  2  3  4  5  6  7 *B  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48
49 50 51 52 53 54 55 56 57 58
```

Sector 12 is no longer in the same place. The remaining bad sector has 11 as a header. If the **slip_sectors** command is reentered and sector 12 is slipped, correctable ECC errors will probably occur on sector 11 in the future.

If only sector 8 is slipped, the following two options are available:

1. Reformat the track which unslips sector 8 and then slip both sectors at one time. Display the track headers before the slip to verify only sector 8 has been previously slipped. If other sectors have been unslipped on this track in the past, slip them also.
2. Check the track headers and then slip the sector which is now in sector 12's place. In this example, slip sector 11.

If sector 12 has been incorrectly slipped, unslip the bad slip by performing option 1.

Display Current Drive and Saved Track

st[atus]

This command lists the Drive Configuration Data (for all selected drives) and displays which drive is the active drive. The **Status** command also displays which track was last saved in the general buffer by one of the commands: **format**, **save_track_data**, or **pattern_test**. In addition, a line is displayed which indicates whether automatic save of track data is enabled (Save is also shown in the prompt).

The following figure shows the information that is displayed when the **status** command is entered:

Figure dev4110–42, *status* Command

```
(D1;Save)-> status

                    DRIVE CONFIGURATION DATA

    IOP MBus MBus  Int   Unit  #    #  Phys  Log
     #   #   CSR  Level   #   Cyl  Hds  Sec  Sec  Name
    --- --- ----- -----  ---  ---  ---  ---  ---  -------
 1.  3   0  0x3f0   2     0   760   19   60   59  DKD-005
 2.  3   0  0x3f0   2     1   760   19   60   59  DKD-005
 3.  3   0  0x3f8   3     0   842   20   46   45  DKD-001

        Drive 1 is currently selected

Saved Track:  drive 3  cylinder 300 head 12

Save of track data is automatic during destructive commands.
(D1;Save)->
```

Switch Between Enable and Disable of Automatic Save

to[ggle_save]

This command switches between enable and disable of automatic save. Automatic save occurs during the commands **format**, **pattern_test**, and **slip_sectors**. The displayed interactive prompt indicates whether automatic save is enabled (`Save`) or disabled (`Nosave`). Also, the **Status** command displays the current setting of automatic save.

Display Sector Numbers

tr[ack_headers_display] *cyl hd* [**to** *cyl hd*]

This command displays the sector numbers for each of the sectors on a track. The first sector number is located physically just after the index so the number is not always zero since sectors are skewed depending on the head number. For example, on head 0, logical sector 0 is the first sector after index, and on head 1, logical sector 0 is the second sector.

Each track has one spare sector (unless it is used because one or more sectors were slipped on the track). The spare sector is marked ***S**. If any sectors have been flagged as bad, they are marked ***B**.

The following figure shows the display of sector numbers for the sectors and a ***S** for a spare sector on a track:

Figure dev4110–43, Displaying Sector Numbers and Spare Sector

```
(D1;Save)-> track 427 2
cylinder = 427  head =  2
58 *S  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22
23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55 56 57
(D1;Save)->
```

In the previous figure, sector 0 is actually the third sector on the track since it is head 2. Also the spare sector (***S**) is just before sector 0.

The following figure shows the display of sector numbers for the sectors and a ***B** for a bad sector on a track:

Figure dev4110–44, Displaying Sector Numbers and Bad Sector

```
(D1;Save)-> track 208 12
cylinder = 208  head = 12
47 48 49 50 51 52 53 54 55 56 57 58  0  1  2  3  4  5 *B  6  7  8  9 10 11
12 13 14 15 16 17 18 19 20 21 22 *B 24 25 26 27 28 *B 30 31 32 33 34 35 36
37 38 39 40 41 42 43 44 45 46
(D1;Save)->
```

In previous figure, three sectors have been flagged bad. The spare sector has been used and sectors 23 and 29 have been relocated and appear in the Bad Block Table (refer to the **bad_block_table** command for more information). Also sector 0 is the 13th sector on the track because this is head 12.

Read a Range of Sectors

v[erify_format] [*nnn* **times**] *cyl hd sec* [**to** *cyl hd sec*]

This command allows repetitive reads of a range of sectors to attempt to detect read errors. The command is not data destructive so it can be used on a customer's disks. It does not perform a data compare since the data is unknown. As the verify progresses, a pass count is incremented on the display to indicate how far the execution has progressed. Any errors are displayed without retry and the reads continue. If any sectors have been relocated, the relocated sectors are read. The argument [**toR** *cyl hd sec*] can be substituted with [**to** *end*]

Execute UNIX Command

! *UNIX-command*

This command is used to issue UNIX commands. After the UNIX command is completed, execution is returned to the interactive prompt.

The following figure shows an example of entering the **!** interactive test command and the **ps** UNIX command:

Figure dev4110–45, Issuing a UNIX Command

```
(D1;Save)-> !ps
   PID TTY TIME CMD
     2 co  0:08 -
   273 co  0:00 dshell
   274 co  0:09 dev4110.t -c 2
   281 co  0:00 sh -c ps?
   282 co  0:02 ps
(D1;Save)->
```

Enter Comments

' comment

This command is used to enter a comment. To enter a comment, type the ' interactive test command followed by a comment.

Disk Parameters File, *DB_diskfmt* Description

The disk parameters file, */mnt/bin/lib/DB_diskfmt*, contains information about disk drives. This information is required to be able to format or test new drives. Each line in the file contains a number of fields separated by one or more spaces. Comments start with a # and continue to the end of the line. Blank lines are also allowed. To add new drives, create a new entry with all the fields defined, and then add the drive to the */ioconfig* file. As of the time of this printing, *DB_diskfmt* contains the following information for all CONVEX machines:

Figure dev4110–46, Contents of the *DB_diskfmt* File

```
# DB_diskfmt - file of disk parameters
# >>>> WARNING - DO NOT USE 'diskfmt' TO FORMAT! It is no longer compatible
# >>>>           with the CONVEX FORMAT! Instead, format MBUS-attached drives
# >>>>           with 'dev4110' and VME-attached drives with 'dev5130'.
# KEY FOR DRIVE NAMES (unformatted capacity is given in parentheses):
#  Name         Description           Name         Description
# DKD-001      Fujitsu Eagle (452MB) DKD-008,208  NEC 2363 (1080MB)
# DKD-002      CDC 9766 (300MB)      DKD-214      Hitachi DK514-38 (356MB)
# DKD-005,206  NEC 2352 (500MB)
#------- XYLOGICS 450/451 SMD CONTROLLER (MBUS) -------
#  a    b   c   d  e  f   g    h    i j k  l  m   n   o  p
DKD-001 2  842 20 46 45 4800 28160 1 0 1  0  0  smd mfm y
DKD-002 0  823 19 32 31 5040 20160 1 0 1  0  0  smd mfm y
DKD-005 0  760 19 60 59 4832 36288 1 0 1  0  0  smd 2-7 y
DKD-008 1 1024 27 68 67 4816 40960 1 0 1  0  0  smd 2-7 y
#------- INTERPHASE 4201 ESDI CONTROLLER (VME) --------
#  a    b   c   d  e  f   g    h    i j k  l  m   n   o  p
DKD-214 0  903 14 51 50 4736 30240 5 5 1  8  8 esdi 2-7 n
#------- INTERPHASE 4200 SMD CONTROLLER (VME) ---------
#  a    b   c   d  e  f   g    h    i j k  l  m   n   o  p
DKD-206 0  760 19 60 59 4832 36288 5 4 1 12 12  smd 2-7 n
DKD-208 0 1024 27 68 67 4816 40960 5 6 1 16 12  smd 2-7 n
# LEGEND:
# a - drive name                Must be DKD-0XX for Multibus and DKD-2XX for
#                               VMEbus
# b - disk type                 For Xylogics controller
# c - # of cylinders
# d - # of heads
# e - # of physical sectors     Number of actual sectors excluding runt
# f - # of logical sectors      Number of physical sectors (e) minus number of
#                               spares
# g - bits per sector           Number of bits between sector pulses
# h - bytes per track           Total number of unformatted bytes per track
# i - skew                      Sector offset from one head to the next
#                               Must be 1 when using Xylogics 450/451 cntlr
# j - # of relocation tracks    .5% of number of cylinders (c). Raise
#                               fractional part to next higher whole number.
#                               Ignored by dev4110 (Multibus formatter)
# k - interleave                sector separation between consecutive sectors
#                               Currently must be 1 for Xylogics 450/451 cntlr
# l - gap 1 size                Number of halfwords in gap before header
#                               (2 bytes per halfword)
#                               Ignored by dev4110 (Multibus formatter)
# m - gap 2 size                Number of halfwords in gap following header
#                               (2 bytes per halfword)
#                               Ignored by dev4110 (Multibus formatter)
# n - drive interface           Used to determine how to read manufacturer's
#                               defect map.  Currently, smd or esdi
#                               Ignored by dev4110 (Multibus formatter)
# o - data encoding scheme      Way data is encoded on the media. Used to
#                               select patterns for pattern test.
#                               Currently mfm, 2-7 or 1-7
# p - Are spares interleaved    For Xylogics, 'y'. For Interphase, 'n'.
```

Diagnostic Cylinder Description

The diagnostic cylinder is located on the first full cylinder preceding the sector forwarding area. Cylinder 840 is the diagnostic cylinder on a Fujitsu Eagle drive, and cylinder 820 is the diagnostic cylinder on a CDC SMD drive.

Each track of the cylinder is independent of the other tracks since there is a "table of contents" stored at sector 0 of each track This table describes what is stored on the remainder of that track. The format of this table is shown below:

Figure dev4110–47, Diagnostic Cylinder Table of Contents Format

```
/* ------------------------------------------------------------------ *
 *              Diagnostic Cylinder Definitions                       *
 * ------------------------------------------------------------------ */
#define NOT_USED        0x00000000      /* position in tbl not used     */
#define NO_HDR          0x00000001      /* this sectors header deleted  */
#define TBL_CONT        0x00000002      /* sector contains tbl of cntnts*/
#define ECC_ERR         0x00000003      /* sector written with bad ecc  */
#define PATTERN         0x00000004      /* sector written with pattern  */

 struct   tbl_cont {
    int   magic_nbr;            /* identifies this as a table of contents */
    int   version;              /* version number of this table */
    int   cyltksc;              /* sector header for this sector*/
    struct {
        int   sec_cont;         /* defines contents of corresponding sector */
        int   pattern;          /* pattern or mask used to verify contents  */
    } sec_tbl[62];
    int   checksum;             /* arithmetic tally of all the above fields */
 };
```

Each track on the cylinder is formatted in such a way that sector 0 is always on the track; sector 0 is written and verified without error when the drive is formatted.

The first field in the table contains the magic number 0x84101500. If this number is not present in the first position of a table, then someone has altered the diagnostic cylinder.

The second field in the table contains the version number. This number is an ordinal number starting with one and increasing as needed. Its purpose is to allow some measure of compatibility of newer diagnostic cylinders with older software. This number is checked if an unknown entry in the sector table (sec_tbl) is encountered. If the version number in the table is greater than the version number of the software, the diagnostic cylinder is assumed to have been formatted with a newer revision of software, and the opcode in the sector table is new to the older software. Therefore, the software is not familiar with the opcode, and the entry in the sec_tbl is ignored.

The next field in the table contains a copy of the sector header (cyltksc) for the table of contents.

The next field in the table contains the sector table (sec_tbl). This table describes what is stored on the rest of the sectors in this track. The sector table consists of 62 entries of 2 int's. Each entry (0 - 61) in this table, corresponds to a sector (0 - 61) on the track. The first position in each entry is the sector contents (sec_cont) field. If the track has more than 62 sectors, the extra sectors are not used or checked by current software. The following table describes what is currently defined:

Table dev4110–9, Defined Values for Sector Contents Field

FIELD	DESCRIPTION
NOT_USED	This sector has not been initialized and should not be checked.
NO_HDR	When this sector is read, the controller should return a 0x05 sector not found error.
TBL_CONT	This sector contains a copy of the table of contents.
ECC_ERROR	This sector contains a copy of the table of contents that has been corrupted to give some form of ECC error. The pattern field contains a mask which may be xor'ed with the magic number field to correct the error. If the mask contains 11 or fewer one bits, the controller should report a soft ECC error when this sector is read. If the mask contains more than 11 one bits, the error reported should be a hard ECC error.
PATTERN	This sector has been filled with the data contained in the pattern field. No errors should be encountered when the sector is read.

The last field in the table of contents is a checksum. This is an arithmetic tally of all the bytes in the table of contents. This value is checked before any of the data in the table of contents is used.

Error Codes

The *dev4110* test reports controller and drive errors in a standard format. However, if additional data is available at the time of the error, it reports that data also. The basic format for the errors is:

```
dev4110 ERROR (Err) ccu/mb/csr/d=c/m/rrr/d Err_desc
```

where:

(*Err*) Identifies the error code associated with the description.

Err_desc Describes the type of error that occurred.

c Gives the CCU slot number for the IOP.

m Is the Multibus chassis number.

rrr Gives the control and status register address (CSR), which identifies the board.

d Specifies the drive number. Each drive begins at 0 with additional drives of the same type being numbered 1, 2, and 3. The number 4 indicates the error occurred while performing a Set Drive Size or NOP command.

If no drive is associated with the error, then the controller and drive information does not appear in the error message.

Additional data may also be reported on a second line (depending on the type of error). For example, the format for data compare errors is:

```
Cyl:dddd Hd:dd
```

The following format appears when errors involve *write*, *read*, *read* and *write HDE*, *read* and *write track headers*, or *seek* commands (depending on the error, the sector number or number of seeks may not appear in the error message):

```
Cyl:dddd Hd:dd Sect:ddd Disp:ddd Exp:hhhh Act:hhhh #Seeks:d
```

where:

Cyl Specifies the position of heads on the drive.

Hd Identifies the head selected.

Disp Identifies number of bytes from the beginning of the sector (data compare errors only).

Exp Specifies the expected value (data compares errors only).

Act Specifies the actual value (data compares errors only).

Sect Indicates the sector where the error occurred.

 # Seeks Identifies the number of seeks executed.

Error Messages

Both *dev4100* and *dev4110* generate the same error codes and report errors in the same format. For details on common error codes and their descriptions, refer to the section entitled **Error messages** in the *dev4100* test description.

Special Error Messages for *dev4110*

In some circumstances, a certain set of error messages are displayed if the peripheral is not powered on, is write protected, or is cabled incorrectly. The test gives the user several options to proceed with, depending on the circumstances. The following examples illustrate these type of error messages and user options that are presented. The first example

illustrates the messages produced when the peripheral is write protected and an operation attempts a write. The second example illustrates the messages produced when the peripheral is not ready (ie., power is not on or a cable is not connected).

> **NOTE**
>
> In the following examples, all **boldface** entries are user entered information.

Figure dev4110–48, Write Protect Error Example

```
(D1;NoSave)-> pattern_test 840 0 30 with aaaaaaaa
     Patterns used:
       aaaaaaaa
pass # 1
dev4110 ERROR (0x14)-ccu/mb/csr/d=3/0/3f0/0 Write-protected disk
  Cyl: 840 Hd: 0 Sect: 30 # Seeks:1
  IOPB: cmd stat  drv hd/s  cyl  cnt addr relo ofst next  ecc eoff
       d100 8514 04a0 001e 4803 0100 0020 0010 0000 0000 0000 0000
Attempt to fix the problem.  You can issue UNIX commands if it helps.
Then enter one of the following:
        <CR> to retry the operation
        'nofix' if unable to fix the problem
UNIX command, <CR> for retry, or nofix: RETURN

dev4110 ERROR (0x14)-ccu/mb/csr/d=3/0/3f0/0 Write-protected disk
  Cyl: 840 Hd: 0 Sect: 30 # Seeks:1
  IOPB: cmd stat  drv hd/s  cyl  cnt addr relo ofst next  ecc eoff
       d100 8514 04a0 001e 4803 0100 0020 0010 0000 0000 0000 0000
Attempt to fix the problem.  You can issue UNIX commands if it helps.
Then enter one of the following:
        <CR> to retry the operation
        'nofix' if unable to fix the problem
UNIX command, <CR> for retry, or nofix: nofix
```

Figure dev4110–49, Drive Not Ready Error Example

```
(D2;Nosave)-> verify_format 0 0 0
             Drive 2: Read of copy #1 of BBT from cyl:759 hd:18 sec:34 failed

dev4110 ERROR (0x16)-ccu/mb/csr/d=7/1/3f0/0 Drive is not ready or faulted
  Cyl: 759 hd:18 Sect: 34
IOPB: cmd stat  drv hd/s  cyl  cnt addr relo ofst next  ecc eoff
     d200 8516 0420 1222 f702 0500 1410 0050 0000 0000 0000 0000
      Drive 2: Read of copy #2 of BBT from cyl:759 hd:18 sec:39 failed

           .
           .
           .

dev4110 ERROR (0x16)-ccu/mb/csr/d=7/1/3f0/0 Drive is not ready or faulted
  Cyl: 759 hd:18 Sect: 49
IOPB: cmd stat  drv hd/s  cyl  cnt addr relo ofst next  ecc eoff
     d200 8516 0420 1231 f702 0500 1410 0050 0000 0000 0000 0000
      Drive 2: Read of copy #5 of BBT from cyl:759 hd:18 sec:54 failed

dev4110 ERROR (0x16)-ccu/mb/csr/d=7/1/3f0/0 Drive is not ready or faulted
  Cyl: 759 hd:18 Sect: 54
IOPB: cmd stat  drv hd/s  cyl  cnt addr relo ofst next  ecc eoff
     d200 8516 0420 1236 f702 0500 1410 0050 0000 0000 0000 0000

dev4110 ERROR (0x4d)-ccu/mb/csr/d=7/1/3f0/0 All copies of BBT are Bad
The internal copy of the BBT is cleared since no good copies were found
Do you want to retry the last operation [yn] -> n
verify_format: pass # 1
dev4110 ERROR (0x4d)-ccu/mb/csr/d=7/1/3f0/0 Drive is not ready or faulted
  Cyl:   0 Hd: 0 Sect:  0 # Seeks:1
  IOPB: cmd stat  drv hd/s  cyl  cnt addr relo ofst next  ecc eoff
       d200 8516 0420 0000 0000 0100 1410 0050 0000 0000 0000 0000

dev4110 ERROR (0x16)-ccu/mb/csr/d=7/1/3f0/0 Drive is not ready or faulted
  Cyl:   0 Hd: 0 Sect:  0 # Seeks:1
  IOPB: cmd stat   drv hd/s  cyl  cnt addr relo ofst next  ecc eoff
Attempt to fix the problem. You can issue UNIX command if it helps.
Then enter one of the following:
        <CR> to retry the operation
        'nofix' if unable to fix the problem
UNIX command, ,CR> for retry, or nofix: RETURN

dev4110 ERROR (0x16)-ccu/mb/csr/d=7/1/3f0/0 Drive is not ready or faulted
  Cyl:   0 Hd: 0 Sect:  0 # Seeks:1
  IOPB: cmd stat   drv hd/s  cyl  cnt addr relo ofst next  ecc eoff
Attempt to fix the problem. You can issue UNIX command if it helps.
Then enter one of the following:
        <CR> to retry the operation
        'nofix' if unable to fix the problem
UNIX command, ,CR> for retry, or nofix: noflx
```

dev4200

Multibus STC Tape Unit Controller Test

Overview

The *dev4200* test verifies the functionality of CONVEX Multibus STC tape controllers.

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test.

Table dev4200–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
IOP	IOP
MBCU	PIA
MBTC[2]	MBCU
Tape Drive	MBTC[2]
	Tape Drive

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

[2] MBTC represents Multibus Tape Controller

Test Invocation

The *dev4200* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4200* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4200–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4200 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4200** executes all *dev4200* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4200–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4200 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev4200–2, Getting Help During Test Parameter Entry

Character	Description
?	Displays this help menu
h	Provides help for a specific prompt
i	Displays the */ioconfig* file

After the desired help information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev4200–3, Test Parameter Menu

```
                ENTER TEST PARAMETERS
      []        Encloses allowed input ranges or values
      ()        Encloses the default value
      ^         Returns to the previous prompt
      :nn       Returns to the prompt # nn
      :         Returns to the first unsatisfied prompt
      :?        Reviews previous entries

                PERIPHERAL CONFIGURATION DATA
       CCU      Chassis  Type    CSR     Int     Unit    Type
       ------   -------  ------  -----   ---     ----    -------
  1)   iop 3      0      MTC-001 0x0c0    4       0      MTD-001
  2)   iop 3      0      MTC-001 0x0c0    4       0      MTD-001

Device 0 = user defined configuration

  1: Device Selection [0,1-2][1]                    (0) ->
  2: IOP [3-7][2]                                  (5) ->
  3: Multibus Chassis [0-3]                        (0) ->
  4: Controller Offset in Multibus [0x0-0xfff]
                                                (0xc0) ->
  5: Controller Interrupt [0-7]                    (4) ->
  6: Tape Unit [0-3]                               (0) ->

         Tape Unit Types:
         0 -> STC 2920
         1 -> STC 1960
         2 -> FUJITSU M2436
         3 -> CDC 92185-04

  7: Tape Unit Type [0-3]                          (0) ->
  8: Media Error Retry Count in Subtests n50-n53 [0-15]
                                                   (5) ->
  9: Display Each Media Error [y,n]                (n) ->
 10: Run Subtests n50-n53 to EOT [y,n]             (n) ->
 11: Fixed Length Block Size, Subtests n10-n12,n30,n50,n51
     [18-131071]                                (512) ->
 12: Run EOT Subtest n25 [y,n]                     (n) ->
 13: Allow Manual Intervention [y,n]               (n) ->
 14: Enter OK, or :NN to return to question NN [OK]
                                                  (OK) ->
```

[1] The options for this prompt change depending on how many tape units are in the system configuration.

[2] The options for this prompt change depending on the machine architecture. For C1 and C120 machines, the available selection ranges from 3-7. For C200 Series machines, the available selection ranges from 0-3.

NOTE

In prompts 8, 10, 11, and 12 in the previous figure, *n* varies from 3 to 5 depending on which classes are executed. Class 3 subtests execute at 800 bpi, Class 4 subtests execute at 1600 bpi, and Class 5 subtests execute at 6250 bpi. Refer to class and subtest descriptions for more information.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

The test parameter prompts are repeated and explained in the following paragraphs.

```
Device Selection [0,1-2]                    (0) ->
```

This prompt selects a device for testing from the system configuration file (*/ioconfig*). If **0** (default) is entered, then user-defined configuration prompts (2-5 in the previous figure) are displayed to determine the configuration to be tested. If a specific device is to be selected, the number of the device is entered (**1**, **2**, etc...). At that point, the additional configuration prompts (2-5 in the previous figure) are not displayed.

```
IOP [3-7]                                   (5) ->
```

Enter the CCU slot number for the desired IOP.

```
Multibus Chassis [0-3]                      (0) ->
```

Enter the number of the chassis to be tested. (The drive is attached to a controller which is in a Multibus chassis.)

```
Controller Offset in Multibus [0x0-0xfff]
                                            (0xc0) ->
```

Enter the low-order 12 bits of the controller's address within the Multibus (this address is selected with switches on the controller).

```
Controller Interrupt [0-7]                  (4) ->
```

Enter the interrupt level of the controller within the Multibus (this is selected with switches on the controller).

```
Tape Unit [0-3]                                    (0) ->
```

Enter the unit number of the tape unit to be tested.

```
Tape Unit Type [0-3]                               (0) ->
```

Enter the number of the type of tape unit to be tested.

```
Media Error Retry Count in Subtests n50-n53 [0-15]
                                                   (5) ->
```

Enter the number of retries to be performed when a media error is detected during Subtests n50–n53.

```
Display Each Media Error [y,n]                     (n) ->
```

Enter **n** or RETURN so media errors and retries are not displayed during all subtests; otherwise, enter **y** to display all media errors and retries during all subtests.

```
Run Subtests n50-n53 to EOT [y,n]                (n) ->
```

Enter **y** to write as many files of data as are required to the end of the tape during Subtests n50–n53.

```
Fixed Length Block Size, Subtests n10-n12,n30,n50,n51
[18-131071]                                     (512) ->
```

Enter (RETURN) to select 512 bytes as the block size of records written to the tape during Subtests n10–n12, n30, n50, n51; otherwise, enter the block size (in bytes) of records written to the tape.

```
Run EOT Subtest n25 [y,n]                        (n) ->
```

Enter **n** or (RETURN) to skip Subtest n25; otherwise, enter **y** to allow execution of Subtest n25, End-of-Tape Sensing.

```
Allow Manual Intervention [y,n]                  (n) ->
```

Enter **n** to skip Subtests 104, 105, 200–202; otherwise, enter **y** to allow execution of Subtests 104, 105, 200–202.

```
Enter OK, or :NN to return to question NN [OK]
                                                (OK) ->
```

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure dev4200–4, Sample Test Parameter Summary

```
                TEST PARAMETER SUMMARY

Device Selection                                    : 0
IOP                                                 : 5
Multibus Chassis                                    : 0
Controller Offset in Multibus                       : 0xc0
Controller Interrupt                                : 4
Tape Unit                                           : 0

        Tape Unit Types:

             0 -> STC 2920
             1 -> STC 1960
             2 -> FUJITSU M2436
             3 -> CDC 92185-04

Tape Unit Type                                      : 0
Media Error Retry Count in Subtests n50-n53         : 5
Display Each Media Error                            : n
Run Subtest n50-n53 to EOT                          : n
Fixed Length Block Size, Subtests n10-n12,n30,n50,n51
                                                    : 512
Run EOT Subtest n25                                 : n
Allow Manual Intervention                           : n
Enter OK, or :NN to return to question NN          : OK
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev4200* test contains the five classes of subtests listed in the following table:

Table dev4200–3, *dev4200* Test Classes

CLASS	DESCRIPTION
1	Controller loopback tests
2	Operator controls tests
3	Functional tests—800 bpi
4	Functional tests—1600 bpi
5	Functional tests—6250 bpi

All of the subtests contained in *dev4200* are loopable under the *dshell*.

Class 1 Subtests

Class 1 subtests verify the basic functionality of the controller. The subtests verify board reset and loopback capabilities. By entering **n** (the default) for the `Allow Manual Intervention` test parameter prompt, Subtests 104 and 105, which require manual intervention are not executed.

Table dev4200–4, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
100	MBTC Reset Capability	00:01
101	MBTC Interrupt Loopback	00:05
102	MBTC Data Loopback	00:25
103	MBTC Memory Access	04:30
104	MBTC Command Loopback	00:10
105	MBTC Chain Command Loopback	00:10

The execution times in the previous table are approximate times for testing a STC 2920 drive at 1600 BPI. Other drives and densities will affect these figures. Specifying a block size larger than the default changes the runtimes for these subtests. All times include rewind time from the tape position at the end of the last subtest.

The *dev4200* test does not test the drive commands: *DMS*, *SNS*, and *LWR*. In addition, it does not test the following controller-error handling capabilities:

- Pending command abort
- Multibus timeout

Also, certain drive capabilities are not tested. This includes all command reject and abort scenarios.

Subtest 100, MBTC Reset Capability

Subtest 100 verifies that the controller resets properly by checking the status register for the correct value.

Subtest 101, MBTC Interrupt Loopback

Subtest 101 verifies that the board interrupt capability can be turned off and on.

Subtest 102, MBTC Data Loopback

Subtest 102 tests the direct memory access First-In-First-Out (FIFO) memory on the board. It pattern checks all RAM's in the FIFO and tests in/out capability, assuming the FIFO operates like a circular buffer with pointers.

Subtest 103, MBTC Memory Access

Subtest 103 checks the capability of the board to access all allowed pages in main memory via the DMA and associated buffers.

Subtest 104, MBTC Command Loopback

Subtest 104 checks the capability of the board to properly register command status for the executing and pending states. This subtest does not execute when **n** (the default) is entered selected for the test parameter prompt `Allow Manual Intervention`.

Subtest 105, MBTC Chain Command Loopback

Subtest 105 checks the capability of the board to properly register command status while executing chaining commands. This subtest does not execute when **n** (the default) is entered for the test parameter prompt `Allow Manual Intervention`.

Class 2 Subtests

Class 2 subtests verify operator controls, tape write protect capability, and unload reel capability. All subtests in this class are skipped if **n** (the default) is entered for the test parameter prompt `Allow Manual Intervention`.

Table dev4200–5, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	MBTC Drive Online	Manual intervention time
201	MBTC Drive Write Protect	Manual intervention time
202	MBTC Drive Unload	Manual intervention time

Subtest 200, MBTC Drive Online

Subtest 200 verifies that drive online status is properly reflected to the software as the operator manipulates the drive controls. This subtest does not execute when **n** (the default) is entered for

the test parameter prompt `Allow Manual Intervention`.

Subtest 201, MBTC Drive Write Protect

Subtest 201 verifies that file protection is properly reflected to the software as the operator removes and reinserts the write ring. This subtest does not execute when **n** (the default) is entered for the test parameter prompt `Allow Manual Intervention`.

Subtest 202, MBTC Drive Unload

Subtest 202 tests the drive unload operation. This subtest does not execute when **n** (the default) is entered for the test parameter prompt `Allow Manual Intervention`.

Class 3, 4, and 5 Subtests

Classes 3, 4, and 5 contain subtests to verify correct operation of the controller and drive for a wide selection of commands and data transfer scenarios, including chaining mode. These subtest are in the range of 300-599 (n00-n99). Subtest numbers in these three classes contain a prefix of *n* (as the hundreds digit), which is used to select tape density. The 300 series subtests are for 800 bpi tapes, 400 series for 1600 bpi, and 500 series for 6250 bpi.

Table dev4200–6, Class 3, 4, and 5 Subtests

SUBTEST	DESCRIPTION
n00[1]	MBTC Write Tape Mark
n01	MBTC File Skip Forward
n02	MBTC File Skip Backward
n03	MBTC Read File Marks Forward
n04	MBTC Read File Marks Backward
n05	MBTC Block Skip File Marks Forward
n06	MBTC Block Skip File Marks Backward
n10	MBTC Write Forward
n11	MBTC Read Forward
n12	MBTC Read Backward
n13	MBTC Block Skip Forward
n14	MBTC Block Skip Backward
n20[1]	MBTC Erase Gap
n25	MBTC End-of-tape Sensing
n30	MBTC Forced Parity Error
n50	MBTC Write Files with Fixed Length Records
n51	MBTC Read Files with Fixed Length Records
n52	MBTC Write Files with Variable Length Records
n53	MBTC Read Files with Variable Length Records
n60	MBTC Write Chained Mode Data Files
n61	MBTC Read Chained Mode Data File

[1] *n* varies from 3 to 5; 3 is 800 bpi, 4 is 1600 bpi, and 5 is 6250 bpi.

The following execution times, which are for an STC 2920 drive at 1600 BPI, are approximate.

Other drives and densities will affect these figures. Specifying a block size larger than the default changes the runtimes for these subtests. All times except *n*00 include rewind time from the tape position at the end of the last subtest. If subtests *n*50-*n*53 are run to the end of the tape, then subtest times are appropriately lengthened, depending on the length of the tape.

Table dev4200–7, Execution Times for $n = 4$

SUBTEST	TIMES (min/sec)
400[1]	00:10
401	00:15
402	00:20
403	00:10
404	00:20
405	00:10
406	00:20
410	00:10
411	00:15
412	00:20
413	00:10
414	00:15
420	00:10
425	time to end of tape
430	01:15
450	01:15
451	02:00
452	02:15
453	03:20
460	02:55
461	02:45

[1] Execution times for the 300 and 500 series subtests vary from those shown for the 400 series.

Subtest n00, MBTC Write Tape Mark

Subtest *n*00 rewinds the tape and then writes a pattern of 100 tape marks. Media errors are ignored unless the count exceeds 5.

> **NOTE**
>
> In this subtest and all the following subtests, *n* varies from 3 to 5 based on tape density; 3 is 800 bpi, 4 is 1600 bpi, and 5 is 6250 bpi.

Subtest n01, MBTC File Skip Forward

Subtest *n*01 rewinds the tape and then uses the file *skip forward* function to skip 90 tape marks written by Subtest *n*00. The subtest ignores media errors unless the count exceeds 10.

Subtest n02, MBTC File Skip Backward

Subtest *n*02 rewinds the tape, skips 90 tape marks written by Subtest *n*00 in the forward direction, and then skips 80 tape marks in the reverse direction. This subtest ignores media errors unless the count exceeds 10 for tape motion in either direction.

Subtest n03, MBTC Read File Marks Forward

Subtest *n*03 rewinds the tape, and then reads 90 tape marks written by Subtest *n*00 with a *block read* function in the forward direction. Media errors are ignored unless the count exceeds 10.

Subtest n04, MBTC Read File Marks Backward

Subtest *n*04 rewinds the tape, uses the *file skip forward* function to skip 90 tape marks written by Subtest *n*00, and reads 80 tape marks backward, using the *block read backward* function. This subtest ignores media errors unless the count exceeds 10 in either direction.

Subtest n05, MBTC Block Skip File Marks Forward

Subtest *n*05 rewinds the tape and then uses the *block skip forward* function to skip over 90 tape marks written by Subtest *n*00. The subtest ignores media errors unless the count exceeds 10.

Subtest n05, MBTC Block Skip File Marks Backward

Subtest *n*06 rewinds the tape, uses the *file skip forward* function to skip 90 tape marks written by Subtest *n*00, and then it skips 80 tape marks backward using the *block skip backward* function. The subtest ignores media errors unless the count exceeds 10 in either direction.

Subtest n10, MBTC Write Forward

Subtest *n*10 rewinds the tape and then writes a data pattern composed of 200 records, each containing incrementing byte values, modulo 256, beginning with zero, followed by 5 tape marks. The number of bytes entered at the test parameter prompt `Fixed Length Block Size` determines the record size; the default record size is 512 bytes. Media errors and block size errors are ignored unless the total count exceeds 10. Errors writing the tape marks are ignored if at least one is valid.

Subtest n11, MBTC Read Forward

Subtest *n*11 first rewinds the tape and then reads forward 190 records written by Subtest *n*10. This subtest ignores media, block size, and data errors unless the total error count exceeds 10.

Subtest n12, MBTC Read Backward

Subtest *n*12 rewinds the tape, skips the pattern written by Subtest *n*10 using the *file skip* function, and then the pattern is read backward for 190 records. The subtest ignores media, block

size, and data errors unless the total error count exceeds 10.

Subtest n13, MBTC Block Skip Forward

Subtest *n*13 rewinds the tape and then skips over 190 tape blocks written by Subtest *n*10 using the *block skip* function. Media errors are ignored unless the error count exceeds 10.

Subtest n14, MBTC Block Skip Backward

Subtest *n*14 rewinds the tape, skips the pattern written by Subtest *n*10 using the *file skip forward* function, and then it skips 190 tape blocks using the *block skip backward* function. Media errors are ignored unless the error count exceeds 10.

Subtest n20, MBTC Erase Gap

Subtest *n*20 rewinds the tape, performs at least 50 erase-gap functions, and then performs a *block skip backward* function. The *block skip backward* function is timed to assure that the long gap exists. The subtest ignores media errors when erasing unless the count exceeds 5.

Subtest n25, MBTC End-of-Tape Sensing

Subtest *n*25 rewinds the tape and performs a *write forward* operation until the EOT marker is read. This subtest executes only when **y** to the `Run EOT Subtest n25` test parameter prompt.

Subtest n30, MBTC Force Parity Error

Subtest *n*30 rewinds the tape and writes a data pattern with the controller set to force parity errors. The forced errors are verified. The subtest ignores media and block size errors unless the total count exceeds 10.

Then the subtest rewinds the tape and a valid data pattern is written without forced errors. Media and block size errors are ignored unless the total count exceeds 10. Then the subtest rewinds the tape again and reads with forced parity errors. The subtest ignores media, block size, and data errors unless the total count exceeds 10.

Subtest n50, MBTC Write Files with Fixed Length Records

Subtest *n*50 rewinds the tape, and then writes 10 files of data patterns. Each file consists of 200 fixed-length data blocks and is terminated with a tape mark. A second tape mark follows the last file. Each data block, which has its length determined by the number entered for the test parameter prompt `Fixed Length Block Size` (default 512 bytes), consists of increasing byte values, modulo 256, beginning with the block number (modulo 256) in the file. The first byte in each block is an exception; it contains the alternating values 0xaa and 0x55. When the end of tape marker is read the first byte contains the value 0xff.

The subtest recovers media errors by using a backspace plus erase gap plus rewrite technique. Any media error is retried the number of times specified in the test parameter prompt `Media Error Retry Count` (the default is 5).

The end of tape causes orderly (but premature) termination of the written data structure compatible with Subtest *n*51. Entering `y` to the test parameter prompt `Run Subtests n50-n53 to EOT` causes the subtest to write as many files of data as are required to fill the tape.

The error statistics which are displayed at the end of the subtest, can also be displayed as the errors occur by entering `y` to the `Display Each Media Error` test parameter prompt.

Subtest n51, MBTC Read Files with Fixed Length Records

Subtest *n*51 rewinds the tape and then reads and verifies the data structure written by Subtest *n*50. The subtest recovers media errors by using a backspace plus reread technique. Any media error is retried the number of times specified for the test parameter prompt `Media Error Retry Count` (default is 5). The subtest detects the end of tape (if any) by reading software marks written by Subtest*n*50.

The error statistics which are displayed at the end of the subtest, can also be displayed as the errors occur by entering `y` to the `Display Each Media Error` test parameter prompt.

Subtest n52, MBTC Write Files with Variable Length Records

Subtest *n*52 rewinds the tape and then writes one file to the tape. The file is terminated with two tape marks. The data in the file consists of records of various lengths, from 18 to 128*1024-1 bytes. Each record contains increasing byte values, modulo 256, beginning with the block size. The first byte in each block is the end of tape marker, which normally has a value of 0xaa. The first byte has a value of zero after the end of tape marker is read.

The subtest recovers media errors by using a backspace plus erase gap plus rewrite technique. Any media error is retried the number of times specified in the test parameter prompt `Media Error Retry Count` (default is 5).

The end of tape causes orderly (but premature) termination of the written data structure compatible with the read Subtest *n*53. If `y` is entered to the test parameter prompt `Run Subtests n50-n53 to EOT`, the subtest writes as many files of data as are required to fill the tape.

The error statistics which are displayed at the end of the subtest, can also be displayed as the errors occur by entering `y` to the `Display Each Media Error` test parameter prompt.

Subtest n53, MBTC Read Files with Variable Length Records

Subtest *n*53 rewinds the tape and then reads and verifies the data structure written by Subtest *n*52. The subtest recovers media errors by using a backspace plus reread technique. The subtest detects the end of tape by reading software marks (if any) written by Subtest *n*52.

The error statistics which are displayed at the end of the subtest, can also be displayed as the errors occur by entering `y` to the `Display Each Media Error` test parameter prompt.

Subtest n60, MBTC Write Chained Mode Data Files

Subtest *n*60 rewinds the tape and then writes one file to the tape. The file consists of several records of various sizes written in chained mode. Two file marks follow the data. The subtest recovers media errors by using a backspace plus erase gap plus rewrite technique. Any media error are retried the number of times specified in the test parameter prompt `Media Error Retry Count` (default is 5).

The error statistics which are displayed at the end of the subtest, can also be displayed by entering `y` to the `Display Each Media Error` test parameter prompt.

Subtest n61, MBTC Read Chained Mode Data File

Subtest *n*61 rewinds the tape and then reads and verifies the data structure written by Subtest *n*60. The subtest recovers media errors by using a backspace plus reread technique. Any media error are retried the number of times specified in the test parameter prompt `Media Error Retry Count` (default is 5).

The error statistics which are displayed at the end of the subtest, can also be displayed by entering `y` to the `Display Each Media Error` test parameter prompt.

Error Messages

Erase Gap Failed
The gap erase function did not succeed in erasing a gap on the tape.

Exception for iop d from recv_iop
{error message detail}
An error has occurred using the SPU/IOP interface to wait for a signal from the IOP that the command is finished. Refer to "Exception from setup_iop" for message detail.

Exception from load_iop
{error message detail}
An error has occurred while bootstrapping the IOP. Make sure that the IOP program image file *dev4200.x00* is available and readable. It must reside either in the current directory or */mnt/test*. Refer to "Exception from setup_iop" for message detail.

Exception from send_iop (*n*)
{error message detail}
An error has occurred using the SPU/IOP interface to signal the IOP that a command is ready. Refer to "Exception from setup_iop" for message detail.

Exception from setup_iop
{error message detail}
An error occurred when preparing to access the IOP. When this error occurs, the message detail may be:

Table dev4200–8, *setup_iop* Exception Error Messages

TEXT	MEANING
HARD ERROR	Hardware error
IOP BUS ERROR	Controller address error
IOP CACHE ERROR	IOP hardware error
IOP PBUS ERROR	IOP hardware error
MMIO ERROR	Main memory error
MULTIBUS ERROR	Hardware error
TIMEOUT	Possible hardware error

Exception from start_iop
{error message detail}
An error has occurred while starting the IOP. Refer to "Exception from setup_iop" for message detail.

Exception in mmalloc_init. Is main memory initialized?
There is a problem accessing main memory. Assure that main memory is present; initialize, if necessary, using *mminit*. If problems persist, consult the Technical Assistance Center.

Function status: message
{UNIX error message or tape drive status dump, if applicable}
There is a problem in IOP processing. The following messages may appear:

Table dev4200–9, IOP Processing Error Messages

TEXT	MEANING
TIME OUT	no response to device command
CHAINING OVERRUN	program and tape drive got out of sync chaining
MEDIA ERROR	tape error

Main memory allocation error
There is a problem allocating main memory. Be sure that main memory is present and initialized. If problems persist, consult the Technical Assistance Center.

MBTC exec level command: *"ccccccccc" (0xnn)*
This message gives a description of the command, where *ccccccccc* is the verbal description of the command.

MBTC exec level command: expected *"ccccccccc" (0xnn)* **actual** *"ccccccccc" (0xnn)*
This message gives the expected and actual command, where *ccccccccc* is the verbal description of the command.

MBTC exec level unit: *nn*

This message gives the unit number in the execution level of the controller.

MBTC exec level unit: expected *nn*, **actual** *nn*

This message indicates a discrepancy in the unit number in the execution level of the controller.

MBTC cstat[1] *0xnn* **means:**

{error message detail}

This indicates a controller error status byte at offset 0x18 of controller. (The error message detail appears in the next entry.)

MBTC cstat[1]: expected *0xnn*, **actual** *0xnn*, **differences:**

{error message detail}

This indicates a discrepancy in the controller status at offset 0x18. The interpretation may be:

```
LAST BYTE [IN]VALID
[NO] MULTIBUS DMA TIMEOUT
[NO] READ PARITY ERROR
[NO] TAPE MARK
PENDING COMMAND [NOT] ABORTED
TAPE ERROR SUMMARY BIT [NOT] SET
```

MBTC cstat[2] *0xnn* **means:**

{error message detail}

This gives the interpretation of the formatter status byte at controller offset 0x19. (Possible interpretations appear in the next message entry.)

MBTC cstat[2]: expected *0xnn*, **actual** *0xnn*, **differences:**

{error message detail}

This message indicates a discrepancy in the formatter status byte at offset 0x19. The error message detail may be:

```
FORMATTER COMMAND [IN]COMPLETE
FORMATTER COMMAND REJECTED
FORMATTER COMMAND ACCEPTED
[NO] DATA OVERRUN
[NO] DATA CHECK
[NO] FORMATTER PROM ERROR
[NO] FORMATTER CORRECTABLE ERROR
[NO] FORMATTER DATA BUS ERROR
```

MBTC exec level density: *ddddd (nn)*

This messages gives the name and number of the density setting.

MBTC exec level density: expected *ddddd (nn)*, **actual** *ddddd (nn)*

This message gives the names and numbers of the expected and actual density.

MBTC dstat[2] *0xnn* **means:**

{error message detail}

This gives the interpretation of the drive status byte at offset 0x22. (The interpretations appear in the next entry.)

MBTC dstat[2]: expected *0xnn*, actual *0xnn*, differences:
{error message detail}

This indicates a discrepancy in the drive status byte at offset 0x22. The message detail may be:

```
DIAG MODE LATCH [NOT] SET
[NO] UCE CONDITION
[NO] WRITE TAPE MARK CHECK
[NO] END DATA CHECK
[NOT] MTE CONDITION
[NO] VEL ERROR
```

MBTC dstat[3] *0xnn* means:
{error message detail}

This gives the interpretation of the drive status byte at offset 0x23. The interpretation may be:

```
[NO] CRC ERROR
```

MBTC dstat[3]: expected *0xnn*, actual *0xnn*, differences:
{error message detail}

This indicates a discrepancy in the drive status byte at offset 0x23. The interpretation may be:

```
[NO] CRC ERROR
```

MBTC dstat[6] *0xnn* means:
{error message detail}

This gives the interpretation of the drive status byte at offset 0x26. (The interpretations appear in the next entry.)

MBTC dstat[6]: expected *0xnn*, actual *0xnn*, differences:
{error message detail}

This indicates a discrepancy in the drive status byte at offset 0x26. The interpretation may be:

```
DRIVE [NOT] READY
DRIVE [NOT] ONLINE
FILE [NOT] PROTECTED
[NOT] AT BEGINNING OF TAPE
[NOT] BACKWARD MOTION
[NOT] HIGH DENSITY
[NOT] PAST END OF TAPE
```

MBTC dstat[7] *0xnn* means:
{error message detail}

This gives the interpretation of the drive status byte at offset 0x27. The message may be:

```
[NOT] WRITE FUNCTION
```

MBTC dstat[7]: expected *0xnn*, actual *0xnn*, differences:
{error message detail}

This indicates a discrepancy in the drive status byte at offset 0x27. The message detail may be:

```
[NOT] WRITE FUNCTION
```

MBTC status *0xnn* means:
{error message detail}

This gives the interpretation of the controller status byte at offset 0x10. The message detail appears in the next entry.

MBTC status: expected *0xnn*, actual *0xnn*, differences:
{error message detail}

This indicates a discrepancy in the controller status byte at offset 0x10. The message detail may be:

```
BLOCK MODE
BUFFER A ACTIVE
BUFFER B ACTIVE
CHAIN MODE
COMMAND [NOT] EXECUTING
COMMAND [NOT] PENDING
DIAGNOSTICS [NOT] ENABLED
FORCE PARITY ERROR
INTERRUPT [NOT] ENABLED
[NO] INTERRUPT REQUEST
USE NORMAL PARITY
```

Pattern error at offset *0xnnnnnn* in buffer: expected *0xnn* actual *oxnn [0xnn 0xnn ...]*

This message indicates an error in data has been detected. The context following the erroneous byte may also be printed.

Retry count for this record: *nn*

This message gives the number of retries required to overcome a media error. This message is generally appended to other messages.

Tape block size error: Expected size: *nn*, actual size: *nn*

This message indicates an erroneous tape block size.

dev4300

Multibus Terminal Controller Test

Overview

The *dev4300* test verifies the functionality of a MTI-800A, MTI-1600A, MTI-850, or MTI-1650 asynchronous communications controller attached through a Multibus chassis to an IOP.

Prerequisites and Required Equipment

In order for this test to run, a Systech controller must be operational. The following table lists the required hardware depending on the type of machine under test.

Table dev4300–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
IOP	IOP
MBCU	MBCU
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Test Invocation

The *dev4300* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4300* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4300–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4300 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4300** executes all *dev4300* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4300–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4300 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev4300–2, Getting Help During Test Parameter Entry

Character	Description
?	Displays this help menu
h	Provides help for a specific prompt
i	Displays the lioconfig file

After the desired help information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev4300–3, Test Parameter Menu

```
                    DEFINE TEST PARAMETERS
     []         Encloses allowed input ranges or values
     ()         Encloses the default value
     ^          Returns to the previous prompt
     :nn        Returns to the prompt # NN
     :          Returns to the first unsatisfied prompt
     :?         Reviews previous entries

       PERIPHERAL CONFIGURATION DATA
      CCU       Chassis  TYPE          CSR     Int
     -------    -------  -------       ---     ---

Device 0 = user defined configuration

 1: Device Selection [0]                          (0) ->
 2: IOP [3-7][1]                                  (5) ->
 3: Multibus Chassis [0-3]                        (0) ->
 4: Controller Offset in Multibus [0x0-0xfff]
                                                (0x20) ->
 5: Controller Interrupt [0-7]                    (7) ->
 6: Port count [8,16]                            (16) ->

    Controller Models

     0) MTI-850/1650
     1) MTI-800/1600

 7: Select Model [0-1]                            (0) ->
 8: Port test Mask (hex), bit 2^n for port n
     [0x1-0xffff]                             (0xffff) ->

    Valid baud rate masks are:
    (Or'ed to get mask)
    8000=  50      4000=  75
    2000=  110     1000=  134.5
    0800=  150     0400=  300*
    0200=  600     0100=  1200*
    0080=  1800    0040=  2000
    0020=  2400*   0010=  3600
    0008=  4800    0004=  7200
    0002=  9600*   0001=  19200*

    * is in default mask

 9: Baud Rate Mask (hex) [0x1-0xffff]         (0x523) ->
10: Are test cables installed?  Enter ? for info
     [y,n,?]                                      (y) ->
11: Enter OK, or :NN to return to question NN [OK]
                                                 (OK) ->
```

[1] The possible selections for this prompt will change depending on machine architecture.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

The test parameter prompts are repeated and explained in the following paragraphs.

```
Device Selection [0,1]                          (0) ->
```

This prompt selects a device for testing from the system configuration. If **0** (default) is entered, then user-defined prompts are displayed to determine the configuration to be tested; otherwise, if a device is selected, the prompts are not displayed.

```
IOP [3-7]                                       (5) ->
```

Enter the CCU slot number for the desired IOP. Then additional prompts are displayed requesting hardware configuration information.

```
Multibus Chassis [0-3]                          (0) ->
```

Enter the number of the chassis to be tested. (The drive is attached to a controller which is in a Multibus chassis.)

```
Controller Offset in Multibus [0x0-0xfff]
                                               (0x20) ->
```

Enter the low-order 12 bits of the controller's address within the Multibus (this address is selected with switches on the controller).

```
Controller Interrupt [0-7]                      (0) ->
```

Enter the interrupt level of the controller within the Multibus (this is selected with switches on the controller).

```
Port count [8,16]                              (16) ->
```

Enter the number of ports per panel. The number of ports per panel depends on the controller model.

```
Select Model [0-1]                              (0) ->
```

Enter the model number of the controller under test.

```
Port test Mask (hex), bit 2^n for port n
[0x1-0xffff]                              (0xffff) ->
```

Enter the mask used to determine which pairs to test during loopback tests. The pairs must be adjacent.

```
Baud Rate Mask (hex) [0x1-0xffff]        (0x523) ->
```

Enter the baud rate to be used to test controllers.

```
Are test cables installed?  Enter ? for info
[y,n,?]                                    (y) ->
```

This prompt is displayed only when the tests to be executed include Class 3 subtests. If **n** is entered to this prompt, the following message is displayed when Class 3 subtests execute:

```
Not executed.  Loopback cables not installed.
```

However, if **y** is entered to the prompt, then the subtests execute normally.

```
Enter OK, or :NN to return to question NN [OK]
                                           (OK) ->
```

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input. If standard output is directed to a disk file, the test parameter summary is also directed to the file.

Figure dev4300–4, Sample Test Parameter Summary

```
                TEST PARAMETER SUMMARY

Device Selection                                        : 0
IOP                                                     : 3
Multibus Chassis                                        : 0
Controller Offset in Multibus                           : 0x20
Controller Interrupt                                    : 7
Port Count                                              : 16

         Controller Models

          0) MTI-850/1650
          1) MTI-800/1600

Select Model                                             : 0
Port Test Mask (hex), bit 2^n for port n                : 0xffff

         Valid baud rate masks are:
         (Or'ed to get mask)
          8000=  50                  4000=  75
          2000=  110                 1000=  134.5
          0800=  150                 0400=  300*
          0200=  600                 0100=  1200*
          0080=  1800                0040=  2000
          0020=  2400*               0010=  3600
          0008=  4800                0004=  7200
          0002=  9600*               0001=  19200*

        * is in default mask

Baud Rate Mask (hex)                                    : 0x523
Are test cables installed?  Enter ? for info            : y
Enter OK, or :NN to return to question NN              : OK
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev4300* test contains three classes of tests shown in the following table.

Table dev4300–3, *dev4300* Test Classes

CLASS	DESCRIPTION
1	Controller basic functional tests
2	Internal loopback tests
3	Physical loopback tests

Where data transmission or modem control testing is to be performed, signal paths between transmitters and receivers are completed by using one of the following methods:

1. Internal loopback on the USARTs
2. Physical loopback between adjacent channels

The first method, internal loopback, which is used in Class 1 and 2 subtests whenever necessary, does not require changing the existing cable connections at the Systech port panel.

> **NOTE**
>
> To run Class 3 subtests, the cables must be disconnected at the ports to be tested and replaced temporarily with test cables, part number 603-030012-200.

Untested commands are those not formally tested in their own subtests. Some of these commands have been used in the construction of subtests for other commands.

Controller commands not formally tested include the following:

- Read USART status register
- Write USART command register
- Abort input
- Abort output
- Suspend output
- Resume output

Class 1 Subtests

Class 1 subtests verify some of the basic functionality of the controller, including, board reset and self-test, firmware level check, timer rate, and internal buffer allocation.

The *dev4300* test contains the following Class 1 subtests, which execute in the times shown:

Table dev4300–4, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
100	Reset and Self-test	:02
101	Firmware Check	:02
102	Timer	:51
103	Buffer Reconfiguration	:14

Subtest 100, Reset and Self-test

Subtest 100 ensures that the controller resets properly by issuing a *reset* command and waiting for the controller to become ready.

Subtest 101, Firmware Check

Subtest 101 checks that firmware revision 3 or newer is installed in the controller. This is accomplished by executing a *read buffered data* command, which is not available in prerevision 3 firmware.

Subtest 102, Timer

Subtest 102 checks the controller timer interrupt rate. An acceptable controller must have at least one rate in the range of 10 to 20 milliseconds. Since the timer interrupt on the controller is not very accurate, the test checks all the timer rates to determine if the controller under test has at lease one rate in the required range. If a valid rate exists, the subtest passes. The actual interrupt rates for the controller under test displays at the completion of the test.

Timer rates are selected by programming the controller with a rate code between 0 and 10 (decimal). Rate codes higher than 10 (decimal) are not used as the interrupt rate is too high.

The nominal timer periods expected depend on the MTI controller model; the time periods are as follows:

Table dev4300–5, MTI Nominal Timer Periods

RATE CODE	ADVERTISED PERIOD (ms)	1600A NOMINAL PERIOD(ms)	1650 NOMINAL PERIOD (ms)
0	530	290	795
1	350	190	525
2	240	130	360
3	200	110	300
4	175	95	263
5	90	50	135
6	45	25	68
7	20	12	30
8	15	8	23
9	13	7	20
10	10	6	15

Subtest 103, Buffer Reconfiguration

Subtest 103 checks the *buffer configuration* command of the controller by picking a channel and configuring one of the sizes from the following table for that channel. This test simultaneously configures all other channels to use all possible remaining buffer space in the controller.

Depending on the port count, the following combinations of legal and illegal buffer sizes (in bytes) are configured:

Table dev4300–6, Buffer Reconfigurations

16 PORT	8 PORT
32	32
40	40
48	48
56	56
15392	15904
15384	15896
15376	15888
15368	15880
0	0
33	33
15400	16002

The test does not attempt block I/O to verify valid configurations.

Class 2 Subtests

Class 2 subtests verify the operation of the controller, using internal loopback when data transfer is necessary.

Table dev4300–7, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	Port Configuration, Internal Loopback	:33
201	Input Channel Configuration, Internal Loopback	:35
202	Output Channel Configuration, Internal Loopback	:05
203	Input Channel Termination Mask, Internal Loopback	:32
204	Modem Configuration, Internal Loopback	:13
205	Single-character Input On/Off, Internal Loopback	:07
206	Block Input, Internal Loopback	:05
207	Block Output, Internal Loopback	:02
220	Single-character Mode, All Patterns, Internal Loopback	:48
221	Single-character Mode, Random Data, Internal Loopback	:51
222	Block Mode, All Patterns, Internal Loopback	:17
223	Block Mode, Random Data, Internal Loopback	:18
224	Block Mode, Various Block Sizes, Internal Loopback	:52

Subtest 200, Port Configuration, Internal Loopback

Subtest 200 checks port configuration programming. Essentially, the test programs the USART mode and command registers to the various configurations as indicated in the following paragraphs. All tests are executed in the internal loopback mode on all ports in the port test mask.

Stop Bit Programming

This test programs the three possible stop bit configurations (1, 1.5, and 2 bits) and 8-bit characters. It passes a block of data at 9600 baud to verify transmission and reception.

Parity Bit Programming

This test programs the three possible parity configurations (none, even, and odd), one stop bit, and 8-bit characters. It passes a block of data at 9600 baud to verify transmission and reception.

Character Length Programming

This test programs the four possible character lengths (5 through 8 bits) and one stop bit. It passes a block of data at 9600 baud to verify transmission and reception.

Baud Rate Programming

This test programs each baud rate specified in the baud rate mask, one stop bit, and 8-bit characters. It passes a block of data at each baud rate to verify transmission and reception.

RTS Assertion Test

Request to Send (RTS) is looped backed to Clear to Send (CTS) by the internal loopback mechanism. The test transmits a block of data with RTS unasserted. Completion should take place only after the USART is reprogrammed to assert RTS.

USART Force Break and Framing Error Test

This test programs a forced break on each port to be tested. It verifies a single null with framing error is received.

DTR Assertion Test

During testing, Data Terminal Ready (DTR) is looped back to Data Carrier Detect (DCD) by the internal loopback mechanism. The test transmits a block of data with DTR unasserted. It verifies completion of output only; input does not complete because DCD is not seen.

USART Transmitter Enable Test

This test programs the USARTs with the transmitter off. Data is looped around, with no response, until the USARTs are reprogrammed to turn on the transmitters.

Four tests (Stop Bit, Parity Bit, Character Length, and Baud Rate) are complemented by Subtest 300, Port Configuration Test which passes data between separate USARTs.

The USART receiver enable test cannot be made. Apparently, the controller firmware turns on the receiver whenever a *receive* command is executed.

Subtest 201, Input Channel Configuration, Internal Loopback

Subtest 201 checks input channel programming on all ports in the port test mask using internal loopback mode. It tests input block and single-character permissions. Termination via ASCII nonprintables and selectable character set is tested. The test does not verify firmware echo and CONTROL-S/CONTROL-Q protocol capabilities.

Subtest 202, Output Channel Configuration, Internal Loopback

Subtest 202 verifies output channel programming, in internal loopback mode, for each port in the port test mask. The block output permission bit is tested to ensure that block output is permitted when programmed and not permitted when not programmed.

Subtest 203, Input Channel Termination Mask, Internal Loopback

Subtest 203 verifies the *input channel termination mask* command. The test also checks the command to ensure that it overrides any termination character selection in the input channel configuration. All tests are conducted in internal loopback mode.

The bytes of the termination masks for each channel are written to sequential numbers, beginning with zero. Then, the test checks the entire mask for proper action of each bit on each input channel.

Subtest 204, Modem Configuration, Internal Loopback

Subtest 204 checks modem change response capability, in internal loopback mode, on all ports in the port test mask. The controller is programmed to return a response when DCD or DSR change, and the response capability for DCD is tested. It ensures that no response is returned when it is not programmed.

Subtest 205, Single-character Input On/Off, Internal Loopback

Subtest 205 checks the individual commands to enable and disable single-character input on all ports in the port test mask. Internal loopback mode is used for all testing.

Subtest 206, Block Input, Internal Loopback

Subtest 206 checks block input termination caused by transmission error and host abort, using internal loopback mode. The test uses *force break* to test transmission error. Host abort is tested by setting up block input and terminating it while pending. Tests are conducted on all ports in the port test mask. (Termination caused by *DMA* error is not tested.)

Subtest 207, Block Output, Internal Loopback

Subtest 207 checks block output termination caused by host abort, using internal loopback mode. Testing is performed by initiating block output at a very low baud rate and then terminating it before it can complete. Tests are conducted on all ports in the test mask. The test does not include *DMA* error response.

Subtest 220, Single-character Mode, All Patterns, Internal Loopback

Subtest 220 performs simultaneous input/output in single-character mode on all tested ports, using internal loopback mode. The test is conducted at all selected baud rates. All possible data patterns are transmitted over each tested port. The test pattern for each port consists of sequentially increasing byte values, modulo 256, beginning with the value of the port number.

The test performs 16 sequential single-character output operations on each output channel. It retrieves 16 single-character responses from each input channel. The process repeats until all 256 patterns are transferred over each channel.

Subtest 221, Single-character Mode, Random Data, Internal Loopback

Subtest 221 performs simultaneous input/output in single-character mode on all tested ports, using random data, in internal loopback mode. The test is conducted at each selected baud rate.

It performs 16 sequential single-character output operations on each output channel and receives 16 single-character responses for each input channel. The process repeats until 256 bytes are transferred over each channel.

Random data is generated using *rand* and *srand*; the seed value is 1309073. The test reinitializes the seed for each baud rate.

Subtest 222, Block Mode, All Patterns, Internal Loopback

Subtest 222 performs simultaneous block mode input/output on all channels to be tested, using internal loopback. The maximum block size used is limited by firmware to 252 bytes. The test is conducted at all selected baud rates.

This subtest passes all possible data patterns through each internally looped back port to be tested. The test pattern for each port is defined to be the sequentially increasing byte values, modulo 256, beginning with the port number.

Subtest 223, Block Mode, Random Data, Internal Loopback

Subtest 223 performs simultaneous block mode input/output on all internally looped back ports to be tested at all selected baud rates. The data block size is arbitrarily fixed at 252 bytes.

This subtest passes pseudo-random data patterns over each port. Random data is generated using the *rand* and *srand* function of the C library; the seed value is 1120597. The test reinitializes the seed for each baud rate.

Subtest 224, Block Mode, Various Block Sizes, Internal Loopback

Subtest 224 performs simultaneous block mode input/output on all ports to be tested, with variable-size blocks, using internal loopback. The test is conducted at all selected baud rates. The data test pattern is random, using a seed value of 137; the test reinitializes the seed at each baud rate. The test uses block sizes 1 through 11, 40, 69, 98, 173, and 252 (the firmware maximum).

Class 3 Subtests

Class 3 subtests verify the correct operation of the controller, using physical loopback cables on ports to be tested.

Table dev4300–8, Class 3 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
300	Port Configuration, Physical Loopback	:12
304	Modem Configuration, Physical Loopback	:13
306	Block Input, Physical Loopback	:02
307	Block Output, Physical Loopback	:03
320	Single-character Mode, All Patterns, Physical Loopback	:48
321	Single-character Mode, Random Data, Physical Loopback	:51
322	Block Mode, All Patterns, Physical Loopback	:18
323	Block Mode, Random Data, Physical Loopback	:17
324	Block Mode, Various Block Sizes, Physical Loopback	:52
330	Continuous Block Input, Read Buffered Data, Physical Loopback	:54
332	Command Error Code Verification, Physical Loopback	:37

Subtest 300, Port Configuration, Physical Loopback

Subtest 300 checks portions of the *port configuration* command, using physical loopback mode. All port pairs in the port test mask are tested. Subtest 300 performs the following tests:

Stop Bit Programming

This test programs the 3 possible stop-bit configurations (1, 1.5, and 2 bits) and 8-bit characters. To verify transmission and reception, it passes a block of data at 9600 baud.

Parity Bit Programming

This test programs the three possible parity configurations (none, even, and odd), one stop bit, and 8-bit characters. It passes a block of data at 9600 baud to verify transmission and reception.

Character Length Programming

This test programs the four possible character lengths (5 through 8 bits) and one stop bit. To verify transmission and reception, the test passes a block of data at 9600 baud.

Baud Rate Programming

This test programs each baud rate specified in the baud rate mask, one stop bit, and 8-bit characters. To verify transmission and reception, it passes a block of data at each baud rate.

Subtest 304, Modem Configuration, Physical Loopback

Subtest 304 checks modem change response capability in physical loopback mode on all port pairs in the port test mask. The controller is programmed to return a response when DCD or DSR change, and the response capability for DCD is tested. It assures that no response is returned when it is not programmed. The test does not include DSR response.

Subtest 306, Block Input, Physical Loopback

Subtest 306 checks block input termination caused by host abort, using physical loopback mode on all port pairs in the port test mask. It tests host abort by setting up block input and terminating it while pending. The test does not check termination caused by transmission error or *DMA* error.

Subtest 307, Block Output, Physical Loopback

Subtest 307 checks block output termination caused by host abort, using physical loopback mode on all port pairs in the port test mask. Testing is performed by initiating block output at a very low baud rate and then terminating it before it can complete. It does not test *DMA* error response.

Subtest 320, Single-character Mode, All Patterns, Physical Loopback

Subtest 320 performs simultaneous input/output in single-character mode on all port pairs to be tested using physical loopback mode. The test performs at all selected baud rates. It transmits all possible data patterns over each tested pair. The test pattern consists of sequentially increasing byte values, modulo 256, beginning with the value of the transmitter port number.

The test performs 16 sequential single-character output operations on each output channel; it receives 16 single-character responses for each input channel. The process repeats until all 256 patterns have been transmitted.

Subtest 321, Single-character Mode, Random Data, Physical Loopback

Subtest 321 performs simultaneous input/output in single-character mode on all tested port pairs, using random data and physical loopback mode. Random data is generated using *rand* and *srand*; the kernel value is 1309073. Tests are conducted at each selected baud rate.

It performs 16 sequential single-character output operations on each output channel, and it receives 16 single-character responses for each input channel. The process repeats until 256 bytes have been transferred over each channel.

Subtest 322, Block Mode, All Patterns, Physical Loopback

Subtest 322 performs simultaneous block mode input/output on all channel pairs to be tested, using physical loopback cables. Firmware limits the maximum block size to 252 bytes. The test is conducted at all selected baud rates.

This subtest passes all possible data patterns over each channel pair to be tested. The test pattern for each port is defined to be the sequentially increasing byte values, modulo 256, beginning with the port number of the transmitter.

Subtest 323, Block Mode, Random Data, Physical Loopback

Subtest 323 performs simultaneous block mode input/output on all channel pairs to be tested, using physical loopback cables. The data block size is arbitrarily fixed at 252 bytes. The test is conducted at each selected baud rate.

This subtest passes pseudo-random data patterns over each channel pair. It generates data bytes using the *rand/srand* function of the C library, using a seed value of 1120597. The seed is reinitialized for each baud rate.

Subtest 324, Block Mode, Various Block Sizes, Physical Loopback

Subtest 324 performs simultaneous block mode input/output on all port pairs to be tested, with variable-size blocks, using physical loopback. The test performs at all selected baud rates. The data test pattern is random, using a seed value of 137, which is reinitialized at each baud rate. The test uses block sizes 1 through 11, 40, 69, 98, 173, and 252 (the firmware maximum).

Subtest 330, Continuous Blk. Input, Read Buffered Data, Phys. Loopback

Subtest 330 performs continuous block input on each of the looped back ports. Each port is tested for its ability to execute the continuous block input at all selected baud rates. The input is terminated by issuing a *read buffered data* command, and the termination cause is verified as well as the data transferred before termination. The amount of data transferred varies according to the baud rate.

Subtest 332, Command Error Code Verification, Physical Loopback

Subtest 332 verifies the firmware's ability to recognize command errors and generate the appropriate error codes. The command errors attempted are: buffer length error, buffer not a multiple of eight (bytes), buffer size greater than 32K (bytes), undefined command nibble, command too short, command too long, channel already configured, input request too big, and output request too big.

Error Messages

Block size error, port *dd*, **expected** *dd*, **actual** *dd*

A data block of the wrong size was received or transmitted. Expected and actual sizes are given.

Command Error Code *0xnn 0xnn*
<message text detailing command error>

Command errors normally result from giving an illegal command to the controller. However, it is possible that controller hardware errors or firmware changes could cause some of these errors. Also, they can be caused by test program errors. Some command errors are:

Table dev4300–9, Command Error Codes

TEXT	MEANING
INPUT REQUEST TOO BIG FOR PORT dd	Possible firmware change
OUTPUT BUFFER FULL FOR PORT dd	Possible firmware change
OUTPUT REQUEST TOO BIG FOR PORT dd	Possible firmware change
PORT dd OFFLINE (SELF-TEST ERROR)	Hardware error
UNKNOWN ERROR STATUS I0xnn	Program/hardware error

Data error, port *dd*, expected *0xnn*, actual *0xnn*

Data verification failed. Expected and actual byte values are given.

Erroneous Block I/O Termination Code, Port *dd*
<message detailing termination code>

The termination cause is incorrect. The termination code displays one of the following messages:

```
TERMINATION CHARACTER
TRANSMISSION ERROR
DMA TO NON-MEMORY
BLOCK COUNT COMPLETE
HOST ABORTED COMMAND
```

Expected and actual values of the termination cause are printed.

Erroneous USART status code
<message detailing status code>

Improper USART status in controller response. The detail of status is:

USART Status Code *0xnn*
<message>

Expected and actual values of the USART status register are printed. The following messages may appear when a USART error occurs:

Table dev4300–10, USART Error Messages

TEXT	MEANING
DSR SENSED	Data set ready sensed
DCD SENSED	Data carrier detected
FRAMING ERROR	Framing error occurred
OVERRUN	Overrun in USART
PARITY ERROR	Parity error detected

Error allocating SPU window map: UNIX error message.

There is a system problem allocating window maps. Contact the Technical Assistance Center.

Error in load_iop
<message detailing error>

An error has occurred while bootstrapping the IOP. Make sure that the IOP program image file *dev4300.x00* is available and readable. It must reside either in the current directory or */mnt/test/*. Refer to "Error in setup_iop" for message detail.

Error in recv_iop
<message detailing error>

An error has occurred using the SPU/IOP interface to wait for a signal from the IOP indicating that the command is finished. Refer to "Error in setup_iop" for message detail.

Error in send_iop
<message detailing error>

An error has occurred using the SPU/IOP interface to signal the IOP that a command is ready to execute. Refer to "Error in setup_iop" for message detail.

Error in setup_iop
<message detailing error>

An error occurred when preparing to access the IOP. When this error occurs, the message may be:

Table dev4300–11, IOP Access Error Messages

TEXT	MEANING
HARD ERROR	Hardware error
IOP BUS ERROR	Controller address error
IOP CACHE ERROR	IOP hardware error
IOP PBUS ERROR	IOP hardware error
MMIO ERROR	Main memory error
MULTIBUS ERROR	Hardware error
TIMEOUT	Possible hardware error

Error in start_iop
<message detailing error>

An error occurred while starting the IOP. Refer to "Error in setup_iop" for message detail.

Error opening device
<message detailing error>

An error occurred while setting up the IOP and device driver to access the requested device. Refer to "Function status" message for more information.

Error opening SPU window to main memory: UNIX error message.

There is a system problem getting access to window map. Contact the Technical Assistance Center.

Exception in mmalloc_int. Is main memory initialized?

There is a problem accessing main memory. Assure that main memory is present; initialize, if necessary, using *mminit*. If problems persist, contact the Technical Assistance Center.

Function status: message
<possible port and channel indication>

There is a problem in IOP command processing. The following messages may appear:

Table dev4300–12, IOP Command Processing Error Messages

TEXT	MEANING
OK	No error
MAIN MEM ALLOC ERROR	Main mem allocation error
IOP NOT OPENED	Open operation failed
INVALID RESPONSE STRING	Controller bad response
CONTROLLER WON'T GO READY	Controller malfunction
NO RESPONSE AVAILABLE	Controller malfunction
ILLEGAL RESPONSE	Controller malfunction
PARTIAL RESPONSE	Controller malfunction
COMMAND ERROR STUCK ON	Controller malfunction
TIMEOUT	Possible controller malfunction
TEST FAILED	Test failed
UNACK'D PBUS INTR	Pbus error
CONTROLLER NOT READY	Controller malfunction

Main memory allocation error

There is a problem allocating main memory. Be sure that main memory is present and initialized. If problems persist, contact the Technical Assistance Center.

Port *dd* unpaired, not tested

This warning appears when running subtests which require adjacent ports to be attached together with special back-to-back cables. When the port test mask (test parameter number 7) does not specify both or neither port in an adjacent pair, the specified port is eliminated from the test.

dev4400

Multibus Line Printer Test

Overview

The *dev4400* test verifies that the Systech MLP-2000 line printer controller and the associated Centronics line printer are online and functional.

Prerequisites and Required Equipment

For this diagnostic to run, a Systech MLP-2000 controller must be resident in a Multibus chassis associated with an IOP. A Systech MLP-2000 line printer controller and Centronics line printer must be operational. The Centronics line printer must be attached to either channel 0 or 1.

The following table lists the required hardware depending on the type of machine under test.

Table dev4400–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
IOP	IOP
MBCU	MBCU
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Test Invocation

The *dev4400* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4400* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4400–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4400 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4400** executes all *dev4400* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4400–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4400 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev4400–2, Getting Help During Test Parameter Entry

Character	Description
?	Displays this help menu
h	Provides help for a specific prompt
i	Displays the */ioconfig* file

After the desired help information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev4400–3, Test Parameter Menu

```
                          ENTER TEST PARAMETERS

              []      Encloses allowed input ranges or values
              ()      Encloses the default value
              ^       Returns to the previous prompt
              :nn     Returns to the prompt # NN
              :       Returns to the first unsatisfied prompt
              :?      Reviews previous entries

               PERIPHERAL CONFIGURATION DATA
     CCU      Chassis Type    CSR     Int     Unit    Type
  -------     ------- ------- -----   ---     ----    ------

Device 0 = user defined configuration

 1: Device Selection [0]                              (0) ->
 2: IOP [3-7][1]                                      (3) ->
 3: Multibus Chassis [0-3]                            (0) ->
 4: Controller Offset in Multibus [0x0-0xfff]
                                                   (0x8c0) ->
 5: Interrupt number [0-7]                            (3) ->
 6: Channel Number [0,1]                              (0) ->
 7: Print Interspace Time (sec) [0-1000]              (0) ->
 8: Enter OK, or :NN to return to question NN  [OK]
                                                     (OK) ->
```

[1] The possible selections for this prompt will change depending on machine architecture.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

Each prompt is repeated and explained in the following section.

```
Device Selection [0,1]                              (0) ->
```

This prompt selects a device for testing from the system configuration file (*/ioconfig*). If **0** (default) is entered, then user-defined configuration prompts (2-5 in the previous figure) are displayed to determine the configuration to be tested. If a specific device is to be selected, the number of the device is entered (**1**, **2**, etc...). At that point, the additional configuration prompts (2-5 in the previous figure) are not displayed.

```
IOP [3-7]                                    (5) ->
```

Enter the CCU slot number for the desired IOP. Then additional prompts are displayed requesting hardware configuration information.

```
Multibus Chassis [0-3]                       (0) ->
```

Enter the number of the chassis to be tested. (The drive is attached to a controller which is in a Multibus chassis.)

```
Controller Offset in Multibus [0x0-0xfff]
                                          (0x8c0) ->
```

Enter the low-order 12 bits of the controller's address within the Multibus (this address is selected with switches on the controller).

```
Interrupt number [0-7]                       (3) ->
```

Enter the interrupt level of the controller within the Multibus (this is selected with switches on the controller).

```
Channel Number [0,1]                         (0) ->
```

Enter **0** if the printer is connected to channel 0 or enter **1** if the printer is connected to channel 1.

```
Print Interspace Time (sec) [0-1000]         (0) ->
```

Enter the amount of time (in seconds) to wait between sending patterns to be printed to the printer.

```
Enter OK, or :NN to return to question NN [OK]
                                            (OK) ->
```

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure dev4400–4, Sample Test Parameter Summary

```
                TEST PARAMETER SUMMARY
Device Selection                                : 0
IOP                                             : 3
Multibus Chassis                                : 0
Controller Offset in Multibus                   : 0x8c0
Interrupt number                                : 3
Channel Number                                  : 0
Print Interspace Time (sec)                     : 0
Enter OK, or :NN to return to question NN       : OK
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev4400* test contains the following class of subtests as shown in the following table:

Table dev4400–3, *dev4400* Test Class

CLASS	DESCRIPTION
2	Pattern print routines

Class 2 Subtests

Class 2 subtests print a rotating character print pattern to the selected line printer. Class 2 subtests are listed in the following table:

Table dev4400–4, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	Rapid Print Pattern	1:00
201	Slow Print Pattern	<:02

Subtest 200, Rapid Print Pattern

Subtest 200 prints 150 consecutive lines of characters. The character pattern is rotated for each line so that each character is tested in each position on the line printer.

Subtest 201, Slow Print Pattern

Subtest 201 prints one line of characters. If subtest looping is enabled, the subtest prompts for a delay between subtest executions which allows for printer adjustment.

Error Messages

At several points in error processing a status dump may take place. A dump may have a status report from the following list:

Ok
No error.

IOP bus error
IOP bus error. Is the Multibus connected to the IOP? Is the controller configured for the correct address? Has the proper controller address been input as a test parameter?

IOP address error
IOP address exception. Should not occur.

IOP cache error
IOP cache error. IOP or controller hardware.

IOP PBUS error
IOP PBUS error. IOP hardware.

Time_out
Operation did not complete properly. May indicate hardware problems with controller or device.

Controller busy
Controller hardware error. Will not return to idle state.

Premature interrupt
Controller hardware error. Premature interrupt.

Inv cmd to IOP
Software error.

Cntlr constant interrupt
Controller hardware error. Constant interrupt.

Controller error
Unexpected controller status.

Multiple interrupts
Controller hardware problem.

Memory alloc error
Internal error.

SPU/IOP req/ack overrun
SPU/IOP intercommunication protocol error.

SPU/IOP PBUS interrupt not acknowledged
SPU/IOP intercommunication error. May be SPU or IOP hardware.

Multibus error
Multibus error interrupt. May be MBCU or controller problem.

User termination
IOP program terminated test. Usually a software problem.

Boot_iop fork error
Internal error.

Boot_iop exit error
Boot IOP problem.

Call error
Software error.

Mmio error
Main memory error. Assure main memory has been initialized.

Error from ipcs_init
Software problem.

Timeout
IOP unresponsive. May be IOP hardware problem.

Hard error
IOP crash. Reason should appear on test output before this error.

In addition, the following error messages may be displayed:

IOP # error: undefined error 9.
This should not occur. If it does, there is a problem in the SPU-Memory-IOP interface.

Line printer 0/1 is offline, not ready, or disconnected.
Line printer is offline, paper is not ready, controller is incorrectly addressed, incorrect channel was selected or incorrect controller was selected.

IOP load failed.
IOP could not be loaded with executable code. Assure that IOP load image resides in current directory or in */mnt/test*.

SPU: Could not find main memory.
Probable cause: main memory not initialized and/or reset.
Fix: run **sysreset** and/or **mminit**.

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dev4410

Multibus Plotter Test

Overview

The *dev4410* test checks the IKON Versatec plotter controller, model 10085, and any attached Versatec plotter.

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test.

Table dev4410–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	MAU
SPU	SP2
IOP	IOP
MBCU	MBCU
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

If a plotter is not available, Class 1 subtests can be run as a check on the IKON controller only. If **y** is entered to the `Test Parameter Instructions` prompt in the test parameter menu, this procedure is described.

Test Invocation

The *dev4410* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4410* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4410–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4410 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4410** executes all *dev4410* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4410–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4410 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev4410–3, Test Parameter Menu

```
                    ENTER TEST PARAMETERS

    []          Encloses allowed input ranges or values
    ()          Encloses the default value
    ^           Returns to the previous prompt
    :nn         Returns to the prompt # nn
    :           Returns to the first unsatisfied prompt
    :?          Reviews previous entries

                    PERIPHERAL CONFIGURATION DATA
     CCU        Chassis Type     CSR     Int     Unit    Type
    -------     ------- -------  -----   ---     ----    --------
 1)  iop 3        0     PRC-002 0x2c0    1

Device 0 = user defined configuration

 1: Device Selection [0,1]                                    (0) ->
 2: IOP [3-7][1]                                              (5) ->
 3: Multibus Chassis [0-3]                                    (0) ->
 4: Controller Offset in Multibus [0x0-0xfff]              (0x2c0) ->
 5: Interrupt Number [0-7]                                    (1) ->
 6: Test Parameter Instructions [y,n]                         (n) ->
 7: Is IKON set for TTL interface [y,n]                       (n) ->
 8: Is IKON set for forced byte mode [y,n]                    (n) ->
 9: Suppress manual intervention [y,n]                        (n) ->

     Plotter models

     0: USER DEFINED                        12: 2000,2030   >64 char
     1:   80                                13: 2160
     2: 200A                 64 char        14: 8122
     3: 200A                >64 char        15: 8222
     4:  800                 64 char        16: 8124
     5:  800                >64 char        17: 8224
     6:  900                                18: 8136
     7: 1100                 64 char        19: 8236
     8: 1100                >64 char        20: 8124
     9: 1200                                21: 8242
    10: 1600                                22: 8172
    11: 2000,2030            64 char

10: Plotter model [0, 1-22]                                   (1) ->
11: Print characters per line [1-1000]                        (0) ->
12: SPP Print chars per line [1-1000]                         (0) ->
13: SPP scan lines for character [1-1000]                     (0) ->
14: Plot bytes per line [1-1000]                              (0) ->
15: Can this plotter print [y,n]                              (y) ->
16: Test ASCII print controls [y,n]                           (y) ->
17: Can this plotter plot [y,n]                               (n) ->
18: Does this plotter have shared print/plot mode
    [y,n]                                                     (y) ->
19: Shorten programmed output plot patterns [y,n]             (n) ->
20: Shorten DMA output plot patterns [y,n]                    (y) ->
21: Self test instructions [y,n]                              (n) ->
22: Enter OK, or :NN to return to question NN [OK]
                                                           (OK) ->
```

[1] The possible selections for this prompt will change depending on machine architecture.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

A description of the meaning of each prompt follows:

```
Device Selection [0,1]                                    (0) ->
```

This prompt selects a device for testing from the system configuration. If the **0** (default) is entered, then user-defined prompts are displayed to determine the configuration to be tested; otherwise, if a device is selected, the prompts are not displayed.

```
IOP [3-7]                                                 (5) ->
```

Enter the CCU slot number for the desired IOP. Then additional prompts are displayed requesting hardware configuration information.

```
Multibus Chassis [0-3]                                    (0) ->
```

Enter the number of the chassis to be tested. (The drive is attached to a controller which is in a Multibus chassis.)

```
Controller Offset in Multibus [0x0-0xfff]                 (0x2c0) ->
```

Enter the low-order 12 bits of the controller's address within the Multibus (this address is selected with switches on the controller).

```
Interrupt Number [0-7]                                    (1) ->
```

Enter the interrupt level of the controller within the Multibus (this is selected with switches on the controller).

The following prompts display one line at a time after the configuration to be tested has been selected:

```
Test Parameter Instructions [y,n]                         (n) ->
```

This prompt allows for the display of a short help file containing information about test strategy and the test parameters.

```
Is IKON set for TTL interface [y,n]                       (n) ->
```

Enter **y** to for TTL (Transistor-Transistor Logic) mode. Most Class 1 subtests (if selected) are

skipped unless TTL mode is selected.

```
Is IKON set for forced byte mode [y,n]                    (n) ->
```

Enter either forced-byte mode or word-mode configuration for the IKON. Generally, word mode is selected.

```
Suppress manual intervention [y,n]                        (n) ->
```

If **y** is entered, Class 1 subtests, which require the plotter to be disconnected, are skipped. In addition, Class 3 subtests (plotter offline and out-of-paper subtests) are skipped. If **n** is entered, instructions such as:

```
Disconnect or reconnect plotter
Put plotter offline or online
Remove or restore plotter paper
```

are displayed when manual functions are performed.

```
Plotter model [0, 1-22]                                   (1) ->
```

If **0** (user-defined plotters) is entered, prompts are displayed for specifying the characteristics of the plotter being used. Entering a value in the range [1-22] causes the user-defined questions to be skipped.

The following four prompts are displayed for user-defined plotters.

```
Print characters per line [1-1000]                        (0) ->
```

Enter the number of characters to print per line.

```
SPP Print chars per line [1-1000]                         (0) ->
```

Enter the number of characters that the plotter can print in a single line when in shared print-plot mode (SPP).

```
SPP scan lines for character [1-1000]                     (0) ->
```

Enter the number of plot scans required to get the entire character block on the output medium.

```
Plot bytes per line [1-1000]                              (0) ->
```

Enter the number of bytes that can be plotted in a single-plot scan on the plotter under test.

```
Can this plotter print [y,n]                              (y) ->
```

Enter whether the plotter being tested has print capability.

```
Test ASCII print controls [y,n]                           (y) ->
```

This prompt is only displayed if **y** is entered to the previous prompt. If the printer has the capability to handle ASCII control characters, enter **y**.

```
Can this plotter plot [y,n]                                    (n) ->
```

If the plotter being tested has plot capability, enter **y**; otherwise, press CTRL for the default.

```
Does this plotter have shared print/plot mode
[y,n]                                                          (y) ->
```

This prompt specifies whether the plotter has shared print-plot mode (print and plot can be overlaid).

```
Shorten programmed output plot patterns [y,n]                  (n) ->
Shorten DMA output plot patterns [y,n]                         (y) ->
```

These prompts allow for shortening the plot-pattern generation. Normally, the full pattern is plotted in programmed output mode, and a short set is plotted in Direct Memory Access (DMA) mode.

```
Self test instructions [y,n]                                   (n) ->
```

Enter **y** to display a help file giving instructions for operating the IKON self-test.

```
Enter OK, or :NN to return to question NN [OK]
                                                              (OK) ->
```

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

After entering all the parameters, the test parameter selections are echoed to the screen. If standard output is directed to a disk file, the test parameter summary is also directed to the disk file.

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev4410* test contains the following three classes of subtests as shown in the following table.

Table dev4410–2, *dev4410* Test Classes

CLASS	DESCRIPTION
1	IKON 10085 controller and loopback tests
2	IKON/Versatec plotter status/interrupt/pattern tests
3	IKON/Versatec plotter offline/no-paper tests

NOTE

The times shown are for the full subtest only (not the shortened version).

Class 1 Subtests

Class 1 subtests verify some of the basic functionality of the controller. Class 1 subtests include board reset and loopback subtests.

Class 1 subtests are listed in the following table:

Table dev4410–3, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
100	IKON Reset Capability	1:40
101	IKON Command Loopback	1:40
102	IKON Plotter Exception Loopback	:26
103	IKON Port Selection	1:40
104	IKON Plotter Mode Selection	1:40
105	IKON Programmed Output Loopback	:11
106	IKON DMA Output Loopback	2:00
107	IKON Data Output Interrupt Capability	:01

Standard ASCII printables are used for print patterns. Plotters may have special characters available for use that are normally considered ASCII control characters. Since some of these characters execute control functions that vary according to user specification, all tests avoid control characters, except for carriage return, newline, form feed, and end-of-transmission. If possible, use a plotter self-test to see all printable characters.

The following describes those items not formally tested:

- Versatec 8xxx series remote toner-on and toner-off commands
- Versatec 8xxx series status signals for low toner supply, toner-on/off status, and data transfer errors
- Versatec 8xxx series ASCII control characters (in print mode) which may be used to turn the toner subsystem on and off
- Serial interface plotters

- ASCII DC1 capability to switch to plot mode
- Option (Centronics) port on the IKON controller

Subtest 100, IKON Reset Capability

Subtest 100 assures that the controller resets properly. This subtest checks the diagnostic command register and status register for the proper values. The controller must generate no interrupt. A plotter does need to be attached for this subtest.

Subtest 101, IKON Command Loopback

Subtest 101 tests the controller command repertoire (remote buffer clear, end-of-line, form feed, end-of-transmission) using an internal loopback mechanism.

Subtest 102, IKON Plotter Exception Loopback

Subtest 102 executes only when the associated test parameters specify this controller as being set for TTL mode and manual intervention is not suppressed. This subtest tests the offline and no-paper exceptions by forcing them through a loopback test mechanism provided for the TTL interface.

Subtest 103, IKON Port Selection

Subtest 103 verifies Versatec versus Option (Centronics compatible) port selection by checking a status bit. The Option port is not tested. A plotter does not need to be attached for this subtest.

Subtest 104, IKON Plotter Mode Selection

Subtest 104 checks that plotter mode selection is properly echoed in the status register. A plotter does not need to be attached for this subtest.

Subtest 105, IKON Programmed Output Loopback

Subtest 105 executes only when the associated test parameters specify this controller as being set for TTL mode and manual intervention is not suppressed.

This subtest performs programmed output of byte patterns, which are checked via the loopback mechanism in the TTL interface. All possible byte patterns are tested by sequentially passing the 256 possible byte values. A random pattern of `0x10001` bytes is tested, using *rand()* and *srand()* with a seed value of 137.

Subtest 106, IKON DMA Output Loopback

Subtest 106 executes only when the associated test parameters specify this controller as being set for TTL mode and manual intervention is not suppressed.

This subtest performs Direct Memory Access (DMA) output of byte patterns, which are checked via the loopback mechanism in the TTL interface. All possible byte patterns are tested by sequentially passing the 256 possible byte values. Many random patterns are tested by using *rand()* and *srand()* with a seed value of 137 plus the buffer size. This subtest tests the following DMA buffer sizes (hex values):

Table dev4410–4, DMA Buffer Sizes

INITIAL SIZE	SIZE INCREMENT	SIZE LIMIT
1	1	10
11	11	100
101	111	ED0
ED1	1	EF0
EF1	101	1000
1001	1001	10000
FFFD	1	10000

Precautions are taken to detect any improper byte swapping by a controller operating in auto-optimizing word mode.

Subtest 107, IKON Data Output Interrupt Capability

Subtest 107 executes only if the associated test parameters specify this controller as being set for TTL mode and manual intervention is not suppressed. This subtest tests the IKON capability to generate an interrupt when output data circuits go idle.

Class 2 Subtests

Class 2 subtests verify correct operation of the controller and plotter combination. Patterns are plotted to verify correct operation. Class 2 subtests are listed in the following table:

Table dev4410–5, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	IKON/Versatec Status Reporting	:19
201	IKON/Versatec Interrupt Reporting	:01
202	IKON/Versatec FF/EOT Busy Check	2:10
210	IKON/Versatec Programmed Output Print	4:40
211	IKON/Versatec DMA Output Print	4:40
220	IKON/Versatec Programmed Output Plot	4:30
221	IKON/Versatec DMA Output Plot	7:35
230	IKON/Versatec Programmed Output Shared	9:00
231	IKON/Versatec DMA Output Shared	12:00

Subtest 200, IKON/Versatec Status Reporting

Subtest 200 verifies the IKON/Versatec capability to generate proper status for conditions "device ready," "device/interface ready," "data output complete." The subtest may plot some unlabeled data; it is to be ignored.

Subtest 201, IKON/Versatec Interrupt Reporting

Subtest 201 verifies the IKON/Versatec capability to generate proper interrupt for conditions "device ready," "device/interface ready," "data output complete." This subtest also tests the capability to force "device ready" internally to the controller. The subtest may plot some unlabeled data; it is to be ignored.

Subtest 202, IKON/Versatec FF/EOT Busy Check

Subtest 202 tests the capability of form feed and end-of-transmission to keep the plotter busy until all previously transmitted data is plotted. Visually verify the plotted output for correctness. Instructions for verification are plotted on the patterns.

Subtest 210, IKON/Versatec Programmed Output Print

Subtest 210 executes only if the associated test parameter specifies that the plotter has print capability. All plotter controls are tested.

The subtest prints test patterns, including interpretation instructions, using programmed output. Visually check all patterns for errors. The test generates the following patterns:

- Rotating pattern of ASCII printable characters
- Sail pattern with X's, using remote line terminate function
- Truncated sail pattern, terminating lines with ASCII newline
- Truncated sail pattern, terminating lines with ASCII carriage return
- Truncated sail pattern, terminating lines with ASCII newline plus carriage return
- Single-line pattern testing remote buffer clear function
- Empty pattern testing remote reset function
- Simple pattern testing remote form-feed function
- Simple pattern testing ASCII form-feed capability
- Simple pattern testing remote end-of-transmission function
- Simple pattern testing ASCII end-of-transmission capability

Only the rotating pattern prints if the shortened programmed output test mode is selected with the associated test parameter. The ASCII control capabilities in the truncated sail patterns, the simple pattern testing ASCII form-feed capability, and the simple pattern end-of-transmission capability are not tested unless requested by the associated test parameter.

Subtest 211, IKON/Versatec DMA Output Print

Subtest 211 executes only if the associated test parameter specifies that the plotter has print capability. The subtest checks all plotter controls.

The test patterns, described in Subtest 210, are printed, using DMA output with interrupt on "device/interface ready." Only the rotating pattern prints the shortened DMA test mode is selected with the associated test parameter.

Subtest 220, IKON/Versatec Programmed Output Plot

Subtest 220 executes only if the associated test parameter specifies that the plotter has plot capability. The subtest checks all plotter controls.

This subtest plots test patterns, including instructions for interpretation, using programmed output. Visually check all patterns for errors. The subtest generates the following patterns:

- Nib-grid pattern (checks each plot nib so that failing nibs may be visually isolated)
- Sail pattern of small bars
- Simple pattern testing remote buffer clear function
- Simple pattern testing remote reset function
- Simple pattern testing remote form-feed function
- Simple pattern testing remote end-of-transmission function

The subtest generates only the nib-grid pattern if the shortened programmed output test mode is selected with the associated test parameter.

Subtest 221, IKON/Versatec DMA Output Plot

Subtest 221 executes only if the associated test parameter specifies that the plotter has plot capability. The subtest checks all plotter controls.

This subtest plots the test patterns, described in Subtest 220, using DMA output with interrupt on "device/interface ready." Only the nib-grid pattern is generated if the shortened DMA test mode is selected with the associated test parameter.

Subtest 230, IKON/Versatec Programmed Output Shared

Subtest 230 executes only if the associated test parameter specifies that the plotter uses shared print/plot mode. The subtest checks all applicable plotter controls.

The subtest patterns are printed/plotted using shared print/plot mode and programmed output. Visually check all patterns for errors; each pattern provides instructions for interpretation. The subtest generates the following patterns in shared plot mode (print buffer empty):

- Nib-grid pattern (checks each plot nib so that failing nibs may be visually isolated)

- Sail pattern of small bars
- Simple pattern testing remote buffer clear
- Simple pattern testing remote reset

The subtest generates the following patterns in shared print mode (using zero-filled plot buffers to scan out the print):

- Rotating pattern of printables
- Sail pattern of X
- Truncated sail pattern of X, using ASCII newline to terminate print buffers
- Truncated sail pattern of X, using ASCII carriage return to terminate print buffers
- Truncated sail pattern of X, using ASCII carriage return plus newline sequence to terminate print buffers
- Empty pattern to test remote buffer clear function
- Empty pattern to test remote reset function

Also, the subtest generates a "close shades on X" pattern, using actual data in both print and plot buffers.

The "truncated sail patterns" (ASCII) are not generated unless enabled by the associated test parameter. Also, only the "close shades on X" pattern is generated when the shortened programmed output test mode is selected with the associated test parameter.

Subtest 231, IKON/Versatec DMA Output Shared

Subtest 231 executes only if the associated test parameter specifies that the plotter uses shared print/plot mode. The test patterns, described in Subtest 230, are printed/plotted using shared print/plot mode and DMA output with interrupt on "device/interface ready." The subtest only generates "close shades of X" pattern when the shortened DMA test mode is selected.

Class 3 Subtests

Class 3 subtests verify correct operation of the controller and plotter when offline and out-of-paper conditions exist. Class 3 subtests are listed in the following table:

Table dev4410–6, Class 3 Subtests

SUBTEST	DESCRIPTION	TIME (minsec)
300	IKON/Versatec Offline Status/Interrupt	N/A[1]
301	IKON/Versatec Out-of-Paper Status/Interrupt	N/A

[1] Manual intervention time

Subtest 300, IKON/Versatec Offline Status/Interrupt

Subtest 300 tests the capability to properly reflect plotter online status and the associated interrupt capability. This subtest does not execute if manual intervention is suppressed with the associated test parameter.

Subtest 301, IKON/Versatec Out-of-paper Status/Interrupt

Subtest 301 tests the capability to properly reflect plotter out-of-paper status. The subtest checks online status, instead, for differential plotters. For TTL plotters, it tests the associated out-of-paper interrupt. This subtest does not execute if manual intervention is suppressed with the associated test parameter.

Error Messages

8259A status: poll | IRR | IMR | ISR *0xnnnnnnnn*

The complete status of the 8259A interrupt controller is presented. The first byte is the poll status; the next, the interrupt request register; the third, the interrupt mask register; and the fourth, the in-service register.

Datum: [**expected** *0xnn*] [**actual** *0xnn*] [**offset** *0xnn*]

This logs a data byte, including expected value, in case of error. The offset, if given, specifies an offset in a data buffer.

Erroneous interrupt
IKON expected interrupt code *0xnn*
{Interpretation}
IKON actual interrupt code *0xnn*
{Interpretation}

An interrupt of one type occurred but an interrupt of another type was expected. Refer to "Missing interrupt" for interpretation detail.

Exception for iop d from recv_iop
{error message detail}

An error has occurred using the SPU/IOP interface to wait for a signal from the IOP that the command is finished. Refer to "Exception from setup_iop" for message detail.

Exception from load_iop
{error message detail}

An error has occurred while bootstrapping the IOP. Make sure that the IOP program image file *dev4410.x00* is available and readable. It must reside either in the current directory or */mnt/test*. Refer to "Exception from setup_iop" for message detail.

Exception from send_iop (n)
{error message detail}

An error has occurred using the SPU/IOP interface to signal the IOP that a command is ready. Refer to "Exception from setup_iop" for message detail.

Exception from setup_iop
{error message detail}

An error occurred when preparing to access the IOP. When this error occurs, the message detail may be:

Table dev4410–7, IOP Access Error Messages

TEXT	MEANING
HARD ERROR	Hardware error
IOP BUS ERROR	Controller address error
IOP CACHE ERROR	IOP hardware error
IOP PBUS ERROR	IOP hardware error
MMIO ERROR	Main memory error
MULTIBUS ERROR	Hardware error
TIMEOUT	Possible hardware error

Exception from start_iop
{error message detail}

An error has occurred while starting the IOP. Refer to "Exception from setup_iop" for message detail.

Exception in mmalloc_init. Is main memory initialized?

There is a problem accessing main memory. Assure that main memory is present; initialize, if necessary, using *mminit*. If problems persist, consult the Technical Assistance Center.

Function status: message
{UNIX error message if applicable}

There is a problem in IOP processing. The following messages may appear:

Table dev4410–8, IOP Processing Error Messages

TEXT	MEANING
UNIX ERROR	Error specified in message
SUBSYSTEM WON'T GO READY	Hardware problem

IKON diag dcmd 0xnn means:
{interpretation of byte}

This logs a diagnostic command loopback byte. (The interpretation appears in the next entry.)

IKON diag dcmd: expected 0xnn, **actual** 0xnn, **differences:**
{interpretation of difference between expected and actual}

The interpretation may be one or more of the following, where the brackets enclose an optional *NOT* indicator:

Figure dev4410–4, Interpreted Error Messages

```
 UN:  UNUSED BITS SET
_VR:  [NOT] VERSATEC RESET
_VC:  [NOT] VERSATEC CLEAR
_VF:  [NOT] VERSATEC FORM FEED
_VT:  [NOT] VERSATEC END OF XMIT
_VL:  [NOT] VERSATEC END OF LINE
```

IKON status 0xnn **means:**
{interpretation}

This is the IKON status byte. The interpretation may be:

Figure dev4410–5, Interpreted Status Byte Error Messages

```
_OP:  VERSATEC PORT
_OP:  OPTION PORT

 DR:  DEV READY (diag)
 DR:  DEV NOT READY (diag)

 IR:  DEV RDY & OUTPUT IDLE
 IR:  DEV BSY | OUTPUT ACTV

 DP:  OUTPUT IDLE
 DP:  OUTPUT ACTIVE

 PL:  PRINT MODE
 PL:  PLOT MODE

 SP:  NOT SHR'D PRT/PLOT
 SP:  SHR'D PRT/PLOT MODE

 OL:  DEV ON LINE
 OL:  DEV OFF LINE

 NP:  DEV NO PAPER
 NP:  DEV HAS PAPER
```

IKON status: expected 0xnn, **actual** 0xnn, **differences:**
{interpretation}

An unexpected status code was obtained. The differences between the actual code and what was desired are interpreted (refer to previous interpretations).

Main memory allocation error

There is a problem allocating main memory. Be sure that main memory is present and initialized. If problems persist, consult the Technical Assistance Center.

Missing interrupt
IKON expected interrupt code *0xnn*
{Interpretation}

An interrupt, which should have occurred, did not occur. The interpretation may be:

Figure dev4410–6, Interpreted Interrupt Error Messages

```
IR0:  DEVICE/INTERFACE READY
IR1:  OUTPUT IDLE
IR2:  DEVICE READY
IR3:  DEVICE OUT OF PAPER
IR4:  DEVICE OFF LINE
```

Spurious interrupt error: *dd* **expected,** *dd* **actual**

The count of spurious interrupts was not as expected. Spurious interrupts are those which are actually 'spurious' (IKON 8259A spurious interrupt) or are extra, but otherwise valid interrupts. (An IKON 8259A spurious interrupt is a condition where the original interrupt cause vanishes before processor interrupt service performs the interrupt acknowledge.)

Unexpected interrupt
IKON actual interrupt code *0xnn*
{interpretation}

An interrupt that was not expected occurred. Refer to "Missing interrupt" for interpretation detail.

dev4500

Multibus Ethernet Controller Test

Overview

The *dev4500* test verifies that the EXOS/201 Ethernet controller board is functional. The test verifies the IOP-to-controller interface and triggers the controller board's built-in self-test.

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test.

Table dev4500–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
IOP	IOP
MBCU	MBCU
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

NOTE

Also, an operational *delni* module must be available for the Class 2 subtests. The *delni* module must be connected to the board under test via CONVEX cable 601-150001-200.

Test Invocation

The *dev4500* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4500* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4500–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4500 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4500** executes all *dev4500* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4500–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4500 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience. For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev4500–2, Getting Help During Test Parameter Entry

Character	Description
?	Displays this help menu
h	Provides help for a specific prompt
i	Displays the */ioconfig* file

After the desired help information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev4500–3, Test Parameter Menu

```
                ENTER TEST PARAMETERS

[]   Encloses allowed input ranges or values
()   Encloses the default value
^    Returns to the previous prompt
:nn  Returns to the prompt # nn
:    Returns to the first unsatisfied prompt
:?   Reviews previous entries

                PERIPHERAL CONFIGURATION DATA
     CCU       Chassis Type    CSR      Int     Unit    Type
     -------   ------- ------- -------  ---     ----    ------
 1)  iop  3       0     LAN-001 0x4c0    1        0      ex

Device 0 = user defined configuration

 1: Device Selection [0,1]                          (0) ->
 2: IOP [3-7][1]                                    (3) ->
 3: Multibus Chassis [0-3]                          (0) ->
 4: Controller Offset in Multibus [0x0-0xfff] (0x0) ->
 5: Controller Interrupt [0-7]                      (0) ->
 6: Subtest loop count [10-1000]                  (100) ->
 7: Transceiver connected to active ethernet? [y,n]
                                                    (y) ->
 8: Enter OK, or :NN to return to question NN [OK]
                                                  (OK) ->
```

[1] The possible selections for this prompt will change depending on machine architecture.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

A description of the meaning of each prompt follows:

```
Device Selection [0,1]                          (0) ->
```

This prompt selects a device for testing from the system configuration. If **0** (default) is entered, then user-defined prompts are displayed to determine the configuration to be tested; otherwise, if a device is selected, the prompts are not displayed.

```
IOP [3-7]                                    (5) ->
```

Enter the CCU slot number for the desired IOP. Then additional prompts are displayed requesting hardware configuration information.

```
Multibus Chassis [0-3]                       (0) ->
```

Enter the number of the chassis to be tested. (The drive is attached to a controller which is in a Multibus chassis.)

```
Controller Offset in Multibus [0x0-0xfff] (0x0) ->
```

Enter the low-order 12 bits of the controller's address within the Multibus (this address is selected with switches on the controller).

```
Controller Interrupt [0-7]                   (0) ->
```

Enter the interrupt level of the controller within the Multibus (this is selected with switches on the controller).

```
Subtest loop count [10-1000]               (100) ->
```

Enter the number of times each subtest is to be repeated.

```
Transceiver connected to active ethernet? [y,n]
                                             (y) ->
```

If **y** is entered, Class 2 subtests are not executed since the subtests require an inactive Ethernet for proper operation.

```
Enter OK, or :NN to return to question NN [OK]
                                            (OK) ->
```

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure dev4500–4, Sample Test Parameter Summary

```
                TEST PARAMETER SUMMARY

Device Selection                              : 0
IOP                                           : 3
Multibus Chassis                              : 0
Controller Offset in Multibus                 : 0x0
Controller Interrupt                          : 0
Subtest loop count                            : 100
Transceiver connected to active ethernet?     : y
Enter OK, or :NN to return to question NN     : OK
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev4500* test contains the following three classes of subtests as shown in the following table:

Table dev4500–3, *dev4500* Test Classes

CLASS	DESCRIPTION
1	EXOS/201 Ethernet controller access test
2	EXOS/201 Ethernet controller functional tests
3	EXOS/201 Ethernet controller online test

Class 1 Subtest

The Class 1 subtest verifies the basic interface from the IOP to the controller. The subtest ensures the controller responds to the IO address expected, and passes an internal self-test. The Class 1 subtest is listed in the following table:

Table dev4500–4, Class 1 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
100	Controller to Host Access	:05

Subtest 100, Controller to Host Access

Subtest 100 verifies basic access paths. The subtest resets the controller board to verify that IOP can access the controller, and that the controller will automatically run a self-test after reset. Next, the IOP commands the controller to configure itself from a table in IOP local memory. This operation tests the controller's ability to access IOP local memory. Then the controller is commanded to configure itself from main memory to test controller-to-main memory access.

Class 2 Subtests

Class 2 subtests verify the ability of the controller to transmit and receive various Ethernet packets. While in the *Ethernet* mode (with the use of a *delni* module connected to the board under test), these subtests transmit packets using an internal "transmit with self-receive" command, and transmit messages to verify the controller's address filtering. The "scatter/gather" operation of the controller is also tested by targeting data blocks to specific memory blocks.

> **NOTE**
>
> The *delni* module must be connected to the board under test via CONVEX cable 601-150001-200.

Each subtest in the 200 series resets and reconfigures the controller at the start of the subtest. This allows the subtests to be run in any order. Each subtest will loop for a user-entered number of passes. Class 2 subtests are listed in the following table:

Table dev4500–5, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	Real Physical Slot Xmit/Recv	:20
201	Modified Physical Slot Xmit/Recv	:20
202	Broadcast Slot Xmit/Recv	:20
203	Real Physical/Broadcast Slot Xmit/Recv	:40
204	Modified Physical/Broadcast Slot Xmit/Recv	:40
205	Foreign Address Rejection Xmit/Recv	1:10
206	Scatter/Gather Operation	:30

Subtest 200, Real Physical Slot Xmit/Recv

Subtest 200 transmits and receives packets sent to the *real* physical address of the controller. (The *real* address slot is the one that is assigned to the board by the manufacturer.)

Subtest 201, Modified Physical Slot Xmit/Recv

Subtest 201 transmits and receives packets sent to the modified physical address of the controller. This operation tests the controller's ability to change the address associated with a given slot, but still transmit and receive Ethernet packets.

Subtest 202, Broadcast Slot Xmit/Recv

Subtest 202 transmits and receives packets sent to the Ethernet broadcast address. Each broadcast packet is received by all controllers on the Ethernet.

Subtest 203, Real Physical/Broadcast Slot Xmit/Recv

Subtest 203 transmits and receives packets sent to the broadcast and physical address of the controller. The subtest transmits both a broadcast and a physical address packet before attempting to receive any packet. This operation checks the controller's ability to "save" packets while waiting for a receive buffer to be supplied by the host computer.

Subtest 204, Modified Physical/Broadcast Slot Xmit/Recv

Subtest 204 transmits and receives packets sent to the broadcast and modified physical address of the controller.

Subtest 205, Foreign Address Rejection Xmit/Recv

Subtest 205 transmits and receives packets sent to the broadcast and physical address of the controller. Another packet address is also sent out to verify that the controller is rejecting packets destined for other controllers.

Subtest 206, Scatter/Gather Operation

Subtest 206 tests for both transmits and receives. The address used is the controller's *real* physical address. This subtest varies the scatter/gather function from 2 blocks to 8 blocks. Each packet is transmitted and received with the same packet split.

Class 3 Subtest

The Class 3 subtest can be executed on an active Ethernet which allows the test to execute without changing the configuration of the hardware. These subtests do not transmit or receive the *broadcast* type Ethernet packets. The Class 3 subtest is listed in the following table:

Table dev4500–6, Class 3 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
300	Real Physical Slot Only Xmit/Recv	:20

Subtest 300, Real Physical Slot Only Xmit/Recv

Subtest 300 only transmits and receives packets on the *real* physical slot. The broadcast slot is disabled. This subtest can be run on an active ethernet without becoming confused by other packets, unless the board is not rejecting packets properly.

Error Messages

When the requested test has completed, a summary displays, using a standard format as shown in the following figure:

Figure dev4500–5, Sample Pass/Fail Printout

```
Subtest 100     0:00:02 passed
Subtest 200     0:00:19 passed
Subtest 201     0:00:19 passed
Subtest 202     0:00:19 passed
Subtest 203     0:00:37 passed
Subtest 204     0:00:37 passed
Subtest 205     0:00:02 failed
```

Whenever an error is detected, an appropriate error message based on the error reporting flags of the *dshell* is displayed as shown in the following figure:

Figure dev4500–6, Sample Error Message

```
*****  Mon Mar  4 17:02:27 1985  *****
Test: dev4500.t  1.1    Class: 2    Subtest: 205 1.1   Count: 1  Error: 0
Failed:  Foreign address rejection xmit/recv test

Error: Unexpected message ID, ID: 0x4b810009, Cmd: 0xd
```

Then an *end message* is displayed in the format shown in the following figure:

Figure dev4500–7, Sample End Message

```
Frames sent/received with no errors          1300/1200
Frames aborted with excess collisions        0
Frames transmitted with heartbeat absent     0
Frames received with alignment errors        0
Frames received with CRC errors              0
Frames lost                                  0

Test 'dev4500.t' failed
Elapsed time:   0:02:17
:
```

dev4510

Multibus HYPERchannel Controller Test

Overview

The *dev4510* test verifies the functionality of an IKON 10077-NSC Hyperchannel controller board. This board interfaces to the Network Systems Corporation (NSC) A400 Hyperchannel Adapter which, in turn, connects to the actual Hyperchannel bus.

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test.

Table dev4510–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
IOP	IOP
MBCU	MBCU
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

NOTE

A loopback cable, CONVEX cable 601-330001-200, is required for Class 2 subtests.

NOTE

The controller board must be detached from the A400 during this test. The voltages must be within margin and the clock must be between 5Mhz and 11Mhz.

This test is *not* designed to verify the IOP or Multibus Control Unit (MBCU). However, the test is coded to protect itself against Multibus or IOP failures if such are encountered.

Test Invocation

The *dev4510* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4510* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4510–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4510 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4510** executes all *dev4510* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4510–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4510 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev4510–2, Getting Help During Test Parameter Entry

CHARACTER	DESCRIPTION
?	Provides the help information
h	Provides help for a specific prompt
i	Displays the */ioconfig* file

After the information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev4510–3, Test Parameter Menu

```
                ENTER TEST PARAMETERS

     []   Encloses allowed input ranges or values
     ()   Encloses the default value
     ^    Returns to the previous prompt
     :nn  Returns to the prompt # nn
     :    Returns to the first unsatisfied prompt
     :?   Reviews previous entries
     ?    Prints an additional help menu

           PERIPHERAL CONFIGURATION DATA
      CCU    Chassis  TYPE    CSR    Int Unit Type
     ------- -------- ------- ------ --- ---- -------
1)   iop 3      0     LAN-002 0xf00  3   0   HYP-001

Enter device 0 to begin user-defined configurations

  1: Device Selection [0,1]                        (0) ->
  2: IOP [3-7][1]                                  (3) ->
  3: Multibus Chassis [0-3]                        (0) ->
  4: Controller Offset in Multibus [0x0-0xfff]
                                                (0x5c0) ->
  5: Interrupt number [0-7]                        (5) ->
  6: Enter OK, or :NN to return to question NN [OK]
                                                  (OK) ->
```

[1] The possible selections for this prompt will change depending on machine architecture.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

A description of the meaning of each prompt follows:

```
Device Selection [0,1]                          (0) ->
```

This prompt allows selection of a controller from the system configuration. If **0** (default) is entered, then user-defined prompts are displayed to determine the configuration to be tested. Otherwise, if a device is entered, the prompts are not displayed.

```
IOP [3-7]                                    (3) ->
```

Enter the CCU slot number for the desired IOP. Then additional prompts are displayed requesting hardware configuration information.

```
Multibus Chassis [0-3]                       (0) ->
```

Enter the number of the chassis to be tested. (The drive is attached to a controller which is in a Multibus chassis.)

```
Controller Offset in Multibus [0x0-0xfff]
                                          (0x5c0) ->
```

Enter the low-order 12 bits of the controller's address within the Multibus (this address is selected with switches on the controller).

```
Interrupt number [0-7]                       (5) ->
```

Enter the interrupt level of the controller within the Multibus (this is selected with switches on the controller).

```
Enter OK, or :NN to return to question NN [OK]
                                            (OK) ->
```

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure dev4510–4, Sample Test Parameter Summary

```
            TEST PARAMETER SUMMARY

IOP                                          : 3
Multibus Chassis                             : 0
Controller Offset in Multibus                : 0x5c0
Interrupt number                             : 5
Enter OK, or :NN to return to question NN    : OK
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed

- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev4510* test contains the following two classes of subtests as shown in the following table:

Table dev4510–3, *dev4510* Test Classes

CLASS	DESCRIPTION
1	IOP/IKON 10077-NSC communications tests
2	IKON 10077-NSC loopback tests

Any subtest may be started by itself. There are no subtest dependencies. However, on an unknown board, it is best to execute all the subtests in their default order since the subtests increase in complexity.

Class 1 Subtests

Class 1 subtests verify the basic interface from the IOP to the controller is functional. This ensures that the IOP can read and write the three control and status registers on the IKON board and reset the board. These tests can be run with or without the loopback switch on (switch 2 of block U26) and with or without the loopback cable. Therefore, the controller can be configured for loopback and then run both classes. Class 1 subtests are listed in the following table:

Table dev4510–4, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
100	Master Clear and ISR/ICR Register Check	0:01
101	Master Clear Through PCR Register	0:01

Subtest 100, Master Clear and ISR/ICR Register Check

Subtest 100 checks basic communications between the IOP and Interface board using the Interface Status Register (ISR) and Interface Control Register (ICR). Basically, values are loaded into the ICR and read back in the ISR.

A master clear is performed through the ICR and verified since the pattern in the ISR after a master clear must be a binary 00X0XXX010000001 where X is an unknown state bit.

Four of the ISR bits can be programmed from the ICR without loopback. These four bits are altered with walking '1's and walking '0's patterns. This operation is repeated 1000 times.

Subtest 101, Master Clear Through PCR Register

Subtest 101 checks that the Pulse Command Register (PCR) can successfully perform a master clear. First, a 4 bit pattern is written to the CYCL, FCN1, FCN2, and FCN3 bits of the ICR and then master clear is pulsed through the PCR. All four bits previously set high should now be low. The master clear is repeated 1000 times with a verify each time.

Class 2 Subtests

Class 2 subtests are performed with the loopback switch of the IKON 10077-NSC board set on (switch 2 of block U26 on the board) and with a loopback cable attached to the board. These loopback features allow most of the board to be tested.

> **NOTE**
>
> A loopback cable, CONVEX cable 601-330001-200, is required for Class 2 subtests.

- Function and status bits in the control and status registers can be verified.
- 16-bit at a time transfers can be performed.
- DMA input and output of blocks of data can be tested.
- Interrupts from the IKON board to the A400 and to the IOP are exercised.

Class 2 subtests are listed in the following table:

Table dev4510–5, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	Verify Programmability of ISR/ICR	0:01
201	Perform 16-bit Transfers	0:02
202	Perform DMA from Main Memory Using ICR	3:50
203	Perform DMA to Main Memory Using ICR	2:05
204	Perform DMA from Main Memory Using PCR	1:45
205	Perform DMA to Main Memory Using PCR	1:00
206	Verify DMA Transfers Without Interrupts	0:10
207	Verify IKON Responds to Attention Interrupt	0:30

Subtest 200, Verify Programmability of ISR/ICR

Subtest 200 performs a more comprehensive test of the ISR/ICR registers using the internal loopback enabled by switch 2 of switch block U26. This test is repeated 1000 times.

Subtest 201 Perform 16-bit Transfers

Subtest 201 performs two-byte transfers with a rotating ones bit and then a rotating zero bit. This operation verifies that each communications line toggles and that there is no crosstalk on the lines. The pattern test is repeated 1000 times.

Subtest 202, Perform DMA from Main Memory Using ICR

Subtest 202 verifies the controller can fetch bytes from main memory and write them to the output port. The last word transferred can be verified by reading the Input Data register (IDR). To ensure that every available window can be read, all windows are allocated and read from. Two bytes are read starting at each window address 0xXXX000 and 0xXXXffe. Then windows are set up for one large area of 64 Kbytes. DMA transfers of varying lengths of 1024, 2048, 4096, etc. bytes up to the 64k limit are performed. Each length of data is repeated for 32 data patterns consisting of walking '1's and walking '0's patterns. The ICR is used to start the DMA transfer.

Subtest 203, Perform DMA to Main Memory Using ICR

Subtest 203 uses the controller's onboard DMA to transfer data to main memory from the Output Data Register (ODR). A two-byte pattern is stored in the ODR and then is written repeatedly to main memory until the entire DMA block has been transferred. DMA transfers vary in length from 1024, 2048, 4096, etc. bytes up to 64 Kbytes. Each length of data is repeated for 32 data patterns consisting of walking '1's and walking '0's patterns. The ICR is used to start the DMA transfer.

Subtest 204, Perform DMA from Main Memory Using PCR

Subtest 204 performs the varying length DMA operation described in Subtest 202 but uses the PCR to start the DMA transfer.

Subtest 205, Perform DMA to Main Memory Using PCR

Subtest 205 is the same as Subtest 203 but uses the PCR to start the DMA transfer.

Subtest 206, Verify DMA Transfers Without Interrupts

Subtest 206 transfers varying lengths of data as in Subtest 202 and waits for the indication in the ISR that each transfer is performed. After the transfer completes, interrupts are also checked to verify none occurred. The DMA flag is then reset and verified that it reset properly. The next transfer then begins.

Subtest 207, Verify IKON Responds to Attention Interrupt

Subtest 207 performs a master clear using the ICR and confirms it was successful by inspecting the results in the ISR. Then it confirms no interrupt is pending and sets FCN2 (a special loopback bit) and IENB (interrupt enable) in the ICR. This operation is supposed to cause an interrupt as if the adapter had sent it. The interrupt is verified.

A second check verifies an ATTN interrupt occurs by inducing it with the loopback bit FCN2 and IENB (interrupt enable). The interrupt is verified.

Troubleshooting Guide

This is a functional test. Standard error reporting routines will report whether a problem is internal or external to the controller board. In addition, many errors have associated with them a list of possible causes that are printed if long error reporting is selected within the dshell (long error reporting is the default). The IKON 10077-NSC Hyperchannel controller board is the only FRU covered by this test.

Interprocessor Protocol

The IOP/SPU communication protocol is supplied by the Message-Based System (MBS).

Error Messages

0x40 Sysreset of ccus and mem failed

The SPU UNIX command *sysreset ccus; sysreset mem* returned a non-zero value. Try the command manually. May require running *io4000* or *mem4000* to isolate the problem.

0x42 IOP print utility memory error

Error in memory access within MBS. IOP-generated output could not be printed.

0x80 Message received on wrong subqueue

Errors 0x80 through 0x83 should never occur. If they do, see the note at the end of this section.

0x81 Wrong subqueue active and locked

Refer to error 0x80.

0x82 Wrong subqueue active and MBS error

Refer to error 0x80.

0x83 Wrong subqueue active, error invalid

Refer to error 0x80.

0x84 Driver executed for no apparent reason

The IOP driver was brought into execution but no reason could be found. Normally, the driver is executed because of a message sent to it from the SPU or because a controller has interrupted the IOP with the correct interrupt signal. Refer to the note at the end of this section.

0x85 Master Clear through the ICR failed

When the master clear bit in the ICR was set, the ISR failed to return to the correct bit pattern. Probably a bad controller.

0x86 Write/read of ISR bits failed

Unable to alter the ISR bits. Probably a bad controller.

0x87 Controller is not present

The IOP received a bus error when attempting to write to the controller's registers. It is most likely the board is not inserted correctly in the Multibus chassis. The controller could be bad.

0x88 Master Clear through the PCR failed

When the master clear bit in the PCR was set, the ISR failed to return to the correct bit pattern. Probably a bad controller.

0x89 Switch 2 of U26 on Cntlr is not ON

An internal loopback was attempted which only succeeds if the described switch is set ON. An internal failure of the controller board is possible.

0x8A Loopback cable is not installed

An external loopback was attempted which only succeeds if the loopback cable is attached properly to both ports of the controller. The cable may be built incorrectly. Refer to the section Prerequisites and Required Hardware for the cable part number. An internal failure of the controller board is possible.

0x8C DMA from memory failed compare

The last two bytes transferred from memory are checked in the IDR for correctness. The compare failed. The failure could be located anywhere along the path from main memory to the controller board, the controller board itself, or the loopback cable.

0x8D DMA to memory failed compare

Refer to error **0x8C.**

0x8E Expected interrupt did not occur

The controller was expected to interrupt in less than 128 msec. No interrupt was detected in this time. Either the interrupt is strapped incorrectly on the board or the board is failing to interrupt when it should.

0x8F Programmed I/O failed data compare

The transmitted and received data from two-byte transfers failed. Either the loopback cable is not working properly, some component along the path from main memory to the controller is malfunctioning, or the controller itself is bad.

0x92 IOP Window Allocation Failed

Setup of a window from the IOP to main memory resulted in an error. Either the IOP or the driver software on the IOP failed. Refer to the note at the end of this section.

0x93 ISR not reset when RDMA & RATN pulsed

At the beginning of several tests, a master clear is performed by pulsing two bits in the ICR or PCR. This message is printed when the ISR is checked afterward and found not to be in a reset state.

0x94 ISR not in proper state after DMA

The ISR is checked after every DMA operation to verify attention is not set (ATTF = 0), DMA is active (DMAF = 1), and ready is true (REDY = 1). One of these conditions was not correct.

0x95 Unexpected interrupt occurred

An interrupt occurred when none was expected. This occurs in Subtests 206 and 207 during portions of the subtests when no interrupt is expected.

0x96 Extended Write/read of ISR bits failed

The test of bits in the ICR and ISR failed because the ISR did not correctly reflect changes made to the ICR.

0xc0 Error when attempting to receive a message

The MBS reported an error in attempting to provide the SPU with a message.

0xc1 Timeout because queue locked

The SPU received a message, but all ten attempts to read the message resulted in the error *MBS queue locked* being reported by the MBS.

0xc2 Msg interrupt but no msg found

The SPU attempted ten times to receive a message when an interrupt occurred, but all attempts failed with a *no message* error from the MBS.

0xc4 Timeout awaiting msg

SPU expected the IOP to send a message, but it did not receive a message. This error message indicates that the controller failed to generate an interrupt when done, or a break exists in the path of the interrupt signal, which prevents it from being detected.

0xc5 Rtn msg from subqueue other than 7

The SPU received a message to the wrong subqueue; all messages are expected to arrive on subqueue seven. Refer to the note at the end of this section.

0xc6 MBS returned bad error code

A call to an MBS routine returned an error code that was unrecognizable.

0xc7 Block transfer routine failed

A memory to memory transfer failed using the function 'blt'. Refer to the note at the end of this section.

0xc8 Too many devices failed. Fail subtest

This message indicates that the test is terminating because the device failure limit was exceeded.

0xc9 Return msg not of valid type

The SPU received a message, but it was not a device result or system error message. Refer to the note at the end of this section.

0xca IOP's queue locked too long

Ten attempts to send a message to the IOP failed, with a locked condition being reported by MBS.

0xcb No room on SPU side for msg from the SPU to the IOP

Ten attempts to send a message failed because no free message MBS blocks were available for the SPU to use.

0xcc Return msg error

An attempt was made to send a message from the IOP to the SPU but resulted in an MBS error being reported by the Message-Based System.

0xcd Error while configuring I/O

The IOP returned a configuration message that specified a controller that does not exist. Refer to the note at the end of this section.

0xcf Too many controllers specified

More than six controllers were specified during user inputs.

0xd0 IOP echoed msg when none sent

The SPU received an echo message, but no message had been sent. Refer to the note at the end of this section.

0xd1 Bad cntlr # in returned msg

A drive result message specified a bad controller number. Refer to the note at the end of this section.

0xd2 Outstanding msg cnt greater than 0

About to start a task in a subtest when a check uncovers that there are still messages expected back from the IOP for the last task. Refer to the note at the end of this section.

0xd3 No msg err when sending to SPU

Ten attempts to send a message from the IOP to the SPU resulted in a in use. Refer to the note at the end of this section.

0xd4 MBS error when sending to SPU

Same as error code 0xd3 except that MBS is reporting an 'MBS_ERROR'.

0xd5 Invalid MBS error when sending to SPU

MBS is failing. It reported back an error code which is invalid. Refer to the note at the end of this section.

0xd6 MBS locked when sending to SPU

Same as error code 0xd3 except that MBS is reporting an 'MBS_LCKD' error.

0xd7 IOP driver device is bad

A request to test an unknown device was sent from the SPU to the IOP. Immediately after the IOP was loaded, it was sent information about the device that was to be tested. However, the latest request to test the device had bad information in it about the device. Refer to the note at the end of this section.

0xd8 MBS error during IOP msg recv

Same as error code 0xd4 except that it occurred during receipt of a message from the SPU to the IOP.

0xd9 MBS queue locked during receive

Same as error code 0xd6 except that it occurred during receipt of a message from the SPU to the IOP.

0xda MBS no message available

Same as error code 0xd3 except that it occurred during receipt of a message from the SPU to the IOP.

0xdb Data chk of echoed msg failed

A data compare of all echoed messages occurs on the SPU. If the compare fails, MBS is having difficulty sending message between the IOP and SPU. A main memory or software error is indicated. Most likely main memory is not working properly so try *mminit* and then rerun. If it still fails, try *mem4000*. Refer to the note at the end of this section.

0xdc Bad message type to get_rtn_msg

A C-function called get_rtn_msg was called to receive an echoed message or the IOP did not properly flag a message so that it looked like an echoed message. On the SPU side, the routine mbs_wait should have been called if an echoed message is actually expected. Refer to the note at the end of this section.

0xdd Processor queue setup failed

A call to the OS system utility, *pqutil*, returned a non-zero value which indicates it failed. Try it manually at the SPU prompt by typing **pqutil -I**. If it fails for any reason, then it cannot initialize memory in the first eight pages of main memory. Try running *mem4000*. If that fails, try reloading */mnt/os* from a backup or release tape and try again. *Dev4100* and *dev4500* also use *pqutil* so maybe try them.

0xde Open for window to main mem failed

An open of the system file */dev/wndw* was attempted and failed. Verify */dev/wndw* exists and has proper permissions.

0xe0 IOP load module (*.x00) not fnd

A check was made of the current directory first and then */mnt/test* for a file called *dev4510.x00*. It was not found. It should exist in */mnt/test*. If it is not there, restore */mnt/test* from a backup or release tape.

0xe1 Error attempting to load iop

A system command to execute *loadccu* failed. First, run *sysreset* and *mminit* and then try it again. If this does not work, try typing **loadccu -3s /mnt/test/dev4510.x00** at the SPU prompt. If this fails, verify */mnt/os/loadccu* exists and has the right permissions. Also verify that */mnt/test/dev4510.x00* has the right permissions.

0xe2 Main memory allocation error

One large block of main memory needs to be allocated by the test on the SPU side but failed. Run *mminit* and then rerun the test. If it still fails, try *mem4000* to verify memory is functional.

NOTES

Certain error messages may indicate a software error. To verify for a software error, perform the following steps:

1. Perform *sysreset* and *mminit -s*.
2. Rerun the failing subtest. If the problem repeats continue with step 3. If no error occurs, record the error in the error log and look for recurrences of the error.
3. Reload */mnt/test* from a backup or release tape. Rerun the failing subtest. If the problem repeats, report it.

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dev4540

Multibus X.25 Controller Test

Overview

The *dev4540* test is a functional test for the CONVEX Multibus X.25 controller. This test attempts to verify that the Multibus X.25 Controller operates properly in the CONVEX Multibus I/O environment.

Specifically, *dev4540* is designed to accomplish the following:

- Verify the functional ability of the Multibus X.25 Controller to operate in the CONVEX Multibus I/O environment. This includes main memory access and interrupt generation.
- Verify that the Multibus X.25 Controller can detect parity errors in the controller's RAM.
- Verify that the Multibus X.25 Controller can transmit and receive data through the on-board Serial Communications Controllers (SCC) via the Direct Memory Access (DMA) controllers.
- Verify that the cable interface and external communications modules are working properly (requires external loopback cables; refer to the "Prerequisites and Required Equipment" section in this chapter for the CONVEX part number).

Channel Control Unit (CCU) communications use the Event Governed Operating System (EGOS) and the Message Based System (MBS) used by ConvexOS. The intent is to test the communication paths that are used in a normal operating environment.

Related Documents

This test description is intended as a reference for users who are familiar with the SBE, Inc. COM-4 board and the operation of the CONVEX I/O system. Additional information on the SBE, Inc. COM-4 board can be found in the *ModulasTen SBE/COM-4 User's Reference Manual* from SBE, Inc.

> **NOTE**
>
> The Multibus X.25 Controller is a modified version of the COM-4 board. Within this test description, COM-4 refers to the Multibus X.25 Controller. Also, any prompts or error messages using COM-4 refer to the Multibus X.25 Controller.

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test.

Table dev4540–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
MIOP	MIOP
MBCU	PIA
Multibus X.25 Controller	MBCU
	Multibus X.25 Controller

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Some subtests (301 and 401) require loopback cables to execute. The following table contains the Serial Communications Interface (SCI) module and the corresponding part numbers for their required loopback cables:

Table dev4540–2, Required Loopback Cables

SCI Type	CONVEX Loopback Cable
RS-232	601-040001-200
RS-449	601-080001-200
V.35	601-060001-200

Test Invocation

The *dev4540* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4540* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user.

> **NOTE**
>
> Use the following test invocation sequence for the initial invocation of *dev4540* or for when the state of the machine is unknown. Also, the following invocation sequence should be used if any hard errors have occurred since the last system initialization.

Figure dev4540–1, Initial Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
:test dev4540 [-c [class number(s)]] [-s [subtest number(s)]] [-option] [-f FILE] [+>filename] RETURN
```

In the previous figure, the prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

> **NOTE**
>
> After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4540** executes all applicable *dev4540* subtests sequentially. To execute a specific class(es) of subtest(s) or one or more individual subtests, use the **-c** or **-s** options during test invocation, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual.

The following list defines the dash options ([*-option*]):

> **NOTE**
>
> In the following list of options, the **-b, -d, -e, -i, -l,** and **-o** options either override the settings specified in the parameter save file (when the test is invoked with the **-q** option or with the **dev4540x** invocation sequence) or the defaults for the prompts in the "Test Parameter Menu."

-V Print the version (build date, or last modification) of this test

-b *rate* Set baud rate for loopback test to *rate*

-d *flgs* Set debug flags to *flgs*

-e *act* Set Multibus X.25 Controller error action to *act*

-f *FILE* Use *FILE* as the parameter save file. If this option is omitted, the parameter file used is */tmp/dev4540.tmp*

-i *iter* Set iteration count to *iter*

-l *line* Select Multibus X.25 Controller line(s) to test

-n Do not actually execute any subtest (used to create a parameter file without actually executing any subtest or display parameter file information with **-q**)

-o *opts* Set external connections to *opts*

-q Quick start-up (use previous parameters from last test invocation — same as **dev4540x**)

-t Execute all applicable subtests sequentially (override parameter file subtest list)

-v Set verbose flag (detailed information printed)

-x *file* Use alternate Multibus X.25 Controller test *file*

The [+>*filename*] option allows the test results to be appended to *filename*.

> **NOTE**
>
> The following alternate test invocation procedure is optimal when invoking *dev4540* multiple times. Using this invocation sequence insures that the test is invoked and executed with all the setup parameters supplied when the test was last executed with the initial invocation sequence.

Figure dev4540–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
:test dev4540x [-c [class number(s)]] [-s [subtest number(s)]] [-option] [-f FILE] [+>filename] RETURN
```

The only difference in this alternate invocation sequence is the **x** after **dev4540**. When invoking *dev4540* in this manner, no prompts are displayed. The diagnostic obtains all prompt information from the parameter file created when the initial invocation sequence was performed. Also note that **mminit -s** and **sysreset** are only required if the state of the machine is unknown or if hard errors have occurred since the last system initialization.

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses appear sequentially on the screen, one line at a time. The figure illustrates *all* questions that can be displayed during test parameter input; however, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially.

Figure dev4540–3, Test Parameter Menu

```
Test 'dev4540.t'              Mon Nov 13 15:27:03 1989

                        ENTER TEST PARAMETERS

        []      Encloses allowed input ranges or values
        ()      Encloses the default value
        ^       Returns to the previous prompt
        :nn     Returns to the prompt # nn
        :       Returns to the first unsatisfied prompt
        :?      Reviews previous entries
        ?       Provides specific help where available

 1: Select ioconfig file [<filepath>,?]            (/ioconfig) -> RETURN

      PERIPHERAL CONFIGURATION DATA
     CCU     Chassis   Type     CSR    Int
    -------- ------- -------- ------ ---
 1) iop  4       0    SCI-001  0x08c0  7
 2) iop  4       0    SCI-001  0x08c2  6
 3) iop  4       1    SCI-001  0x08c0  7
 4) iop  4       1    SCI-001  0x08c2  6

                      *** Enter 0 for manual configuration ***

 2: Ioconfig File Unit to Test [1-4,0,?]                    (1) -> 0
 3: Multibus IOP Number [3-7,?]                             (4) -> RETURN
 4: Multibus Chassis Number [0-1,?]                         (0) -> RETURN
 5: Multibus CSR of the Controller [0x0-0xffe,?]       (0x8c0) -> RETURN
 6: Multibus Interrupt Level of the Controller [0-7,?]      (7) -> RETURN
 7: Use Defaults for Remaining Parameters [y,n,?]           (y) -> n
 8: RAM Pattern Subtest: pattern # 1 [<pattern>,?]
                                    (Use default patterns) -> 01234567
 9: RAM Pattern Subtest: pattern # 2 [<pattern>,?]
                                    (Use default patterns) -> 89abcdef
10: RAM Pattern Subtest: pattern # 3 [<pattern>,?]
                                    (Use default patterns) -> RETURN

       ** External Connections (bit mapped) **
    0x0001: Loopback jumper is installed
    0x0002: Transmit clock source (1=DCE,0=DTE)
    0x0004: Modem is attached to connector

11: Select External Connections [0x0-0x7,?]              (0x2) -> RETURN
12: Select Serial Communication Lines [0x1-0xf,?]        (0xf) -> RETURN
13: Baud Rate for Loopback Subtests [110-73728,?]     (57600) -> RETURN
14: Number of Iterations for Each Subtest [1-2147483647,?]
                                                           (1) -> RETURN
```

Figure dev4540–3, Test Parameter Menu (continued)

```
        ** Debug Mode Flags (bit mapped) **
    0x0001: Print messages sent to COM-4
    0x0002: Print messages received from COM-4
    0x0004: Pause before message sent to COM-4
    0x0008: Pause after message received from COM-4
    0x0010: Print MBS messages sent to CCU
    0x0020: Print MBS messages received from CCU
    0x0040: Pause before MBS message sent to CCU
    0x0080: Pause after MBS message received from CCU
    0x0100: Print extra informative messages
    0x0200: Don't reset COM-4 after subtest is aborted
    0x0400: Don't disable SPU interrupts when done
    0x0800: Simulate all MBS messages (don't send them)

15: Select Debug Mode [0x0-0xfff,?]                    (0x0) -> (RETURN)

        ** Subtest Error Actions **
    1:  Silently ignore subtest errors
    2:  Pause for subtest errors
    3:  Abort subtest on first error

16: Select COM-4 Subtest Error Action [1-3,?]            (2) -> (RETURN)

        ** Error Start/Finish Text Options (bit mapped) **
    0x0001: Enable error start text
    0x0002: Enable error finish text

17: Select Error Start/Finish Message Mode [0x0-0x3,?]  (0x0) -> 0x3
18: Error Start Character Sequence [<error start string>,?]
                                                  (\033[?5i) -> (RETURN)
19: Error Finish Character Sequence [<error finish string>,?]
                                                  (\033[?4i) -> (RETURN)
20: Enter OK, or :NN to return to question NN [OK]       (OK) -> OK
```

If **OK** or (RETURN) is entered, the "Test Parameter Menu" terminates and all inputs are no longer changeable.

For help or information during test parameter entry, enter one of the following characters followed by a (RETURN):

Table dev4540–3, Getting Help During Test Parameter Entry

Character	Description
:?	Reviews previous entries
?	Provides specific help where available

After the desired help information displays, the system redisplays the last prompt.

When all prompts are answered, the screen displays a TEST PARAMETER SUMMARY which displays the prompts that were answered and their responses. The following figure illustrates an example of a TEST PARAMETER SUMMARY screen. The actual values and responses vary according to the input.

Figure dev4540–4, Sample Test Parameter Summary

```
                    TEST PARAMETER SUMMARY

Select ioconfig file                                    : ioconfig
Ioconfig File Unit to Test                              : 0
Multibus IOP Number                                     : 4
Multibus Chassis Number                                 : 0
Multibus CSR of the Controller                          : 0x8c0
Multibus Interrupt Level of the Controller              : 7
Use Defaults for Remaining Parameters                   : n
Select External Connections                             : 0x0002
          -> Transmit clock source (1=DCE,0=DTE) <-
Select Serial Communication Lines                       : 0xf
Baud Rate for Loopback Subtests                         : 57600
Number of Iterations for Each Subtest                   : 1
Select Debug Mode                                       : 0x0000
Select COM-4 Subtest Error Action                       : 2
        -> Pause for subtest errors <-
Select Error Start/Finish Message Mode                  : 0x0003
        -> Enable error start text <-
        -> Enable error finish text <-
Error Start Character Sequence                          : \033[?51
Error Finish Character Sequence                         : \033[?41
Enter OK, or :NN to return to question NN               : OK
```

Initialization Sequence for *dev4540*

After the last prompt is entered, when not in quick start-up mode, and before subtest code execution begins, the following events occur:

- The diagnostic determines if the test was invoked for quick start-up (i.e., **dev4540x** or **dev4540 -q**). If so, the diagnostic reads the test parameters from the specified parameter file (default parameter file is */tmp/dev4540.tmp*). If not, the input parameters are written to the parameter file (default or user specified).
- The diagnostic checks to see if the CCU is already loaded with the *dev4540* CCU driver. If the driver is not loaded, the CCU is loaded. After the load completes, the driver is configured for EGOS and then the EGOS probe message starts the driver.

> **NOTE**
>
> The file */mnt/boot_db* is used to determine what memory is installed. If this file is nonexistent, it can be created with the command: **scn_util -b > /mnt/boot_db** from the **(spu)>** prompt.

After all the above events have occurred, the test code is started.

Prompt Explanations

The test parameter prompts are repeated and explained in the following paragraphs.

```
1: Select ioconfig file [<filepath>,?]          (/ioconfig) ->
```

This option allows specification of an alternate */ioconfig* file. The file must still be in the same format as a conventional */ioconfig* file.

```
      PERIPHERAL CONFIGURATION DATA
       CCU     Chassis    Type     CSR    Int
    -------- ---------- -------- ------ ---
1)  iop  4        0     SCI-001  0x08c0  7
2)  iop  4        0     SCI-001  0x08c2  6
3)  iop  4        1     SCI-001  0x08c0  7
4)  iop  4        1     SCI-001  0x08c2  6

        *** Enter 0 for manual configuration ***

2: Ioconfig File Unit to Test [1-4,0,?]                (1) ->
```

Above, the applicable */ioconfig* file entries are listed (if any). To select a predefined controller configuration entry from the */ioconfig* file, enter the number which is found to the left of the desired entry. Entering a **0** allows each item within the controller configuration entry to be independently specified. The default values are initially the same as the first file entry. If most, but not all, the items associated with a given entry in */ioconfig* file are desired, select the number for that entry, back up to this prompt (via the ^ command), and specify **0** the second time. This changes the default values for the independent items to be the same as the originally selected entry.

```
3: Multibus IOP Number [3-7,?]                         (4) ->
```

Enter the CCU slot number for the Multibus IOP which controls the Multibus chassis containing the Multibus X.25 Controller.

```
4: Multibus Chassis Number [0-1,?]                     (0) ->
```

Enter the Multibus chassis number for the chassis where the Multibus X.25 Controller is installed. If there is only 1 chassis, the number is most likely 0.

```
5: Multibus CSR of the Controller [0x0-0xffe,?]      (0x8c0) ->
```

Enter the Multibus address of the Multibus X.25 Controller Status Register (CSR). This address is controlled by jumper block J28 on the controller. The standard address is 0x8c0. The following tables contain the address and jumper designations for jumper block J28 (near the Multibus edge connector P1). Also the standard address and interrupt levels for jumper blocks J28 and J37 are listed. The information contained in these tables can be viewed online by entering **?** in response to the prompt.

Table dev4540–4, Jumper Block J28 Address and Jumper Designations

JUMPER BLOCK J28							
Address:	A7	A6	A5	A4	A3	A2	A1
Jumper:	1	2	3	4	5	6	7

Table dev4540–5, Standard Address and Interrupt Levels (J28, J37):

X.25 #	Address	Interrupt Level	Jumper J28 1234567	Jumper J37 123456789X
1	0x8c0	7	1100000	XX
2	0x8c2	6	1100001	X X

NOTE

In the previous table, the Xs under the J37 column indicate jumper pins on the J37 jumper that should be connected together.

```
6: Multibus Interrupt Level of the Controller [0-7,?]    (7) ->
```

Enter the CONVEX Multibus interrupt number assigned to the Multibus X.25 Controller under test. This value is between 0 and 7, inclusive. The interrupt level is selected by jumper block J37 (next to Multibus edge connector P1) on the controller. The standard level is 7. The following table lists the pin/interrupt levels and the standard address/interrupt levels for jumper blocks J37 and J28. The information contained in the following tables can also be viewed online by entering **?** as a response to the prompt.

NOTE

Identify the desired interrupt level in the following table and connect the corresponding pin to J37 pin 10. For example, if the desired interrupt level is 2, connect J37 pin 4 to J37 pin 10.

Table dev4540–6, Jumper Block J37, Pin and Interrupt Levels

JUMPER BLOCK J37								
J37 Pin:	2	3	4	5	6	7	8	9
Interrupt Level:	0	1	2	3	4	5	6	7

Table dev4540–7, Standard Address and Interrupt Levels (J28, J37):

X.25 #	Address	Interrupt Level	Jumper J28 1234567	Jumper J37 123456789X
1	0x8c0	7	1100000	XX
2	0x8c2	6	1100001	X X

NOTE

In the previous table, the Xs under the J37 column indicate jumper pins on the J37 jumper that should be connected together.

```
7: Use Defaults for Remaining Parameters [y,n,?]          (y) ->
```

Enter **y** to select the default values for all remaining prompts. This avoids explicit entry of RETURN in response to remaining prompts.

```
8: RAM Pattern Subtest: pattern # 1 [<pattern>,?]
                                    (Use default patterns) ->
9: RAM Pattern Subtest: pattern # 2 [<pattern>,?]
                                    (Use default patterns) ->
10: RAM Pattern Subtest: pattern # 3 [<pattern>,?]
                                    (Use default patterns) ->
```

Select the pattern(s) to use for RAM pattern testing. Patterns are specified by typing the hexadecimal pattern (up to 8 hexadecimal digits). More than one pattern may be entered by entering the pattern, pressing RETURN, and entering another pattern. This process may be continued until the desired number of patterns are entered. When all patterns are entered, press RETURN without typing a pattern. There is a limit of 32 patterns.

```
    ** External Connections (bit mapped) **
0x0001:   Loopback jumper is installed
0x0002:   Transmit clock source (1=DCE,0=DTE)
0x0004:   Modem is attached to connector

11: Select External Connections [0x0-0x7,?]              (0x2) ->
```

This prompt controls whether or not the diagnostic allows use of an external loopback jumper. External loopback provides a cable check to the external connector panel, while internal loopback does not check any external cables. The external connections affect which Class 3 and Class 4 subtests are executed. The following list specifies which subtests require which of these options:

- Subtest 300—requires options 2 and 4 to be set (0x6 or 0x7)
- Subtest 301—requires options 1 and 2 to be set (0x3 or 0x7)
- Subtest 400—requires options 4 to be set and 2 to be clear (0x4 or 0x5)
- Subtest 401—requires options 1 to be set and 2 to be clear (0x1 or 0x5)

If the value selected is not one of the values contained in the previous list, no class 3 or class 4

subtests are executed. The selection of external connections may also be set by using the **-o** command line option during the test invocation sequence.

```
12: Select Serial Communication Lines [0x1-0xf,?]        (0xf) ->
```

Select which lines to test. Normally all lines are tested. This prompt allows testing on a subset of the lines. Lines are specified as a bitmask, with the least significant bit corresponding to line 1. The selection of serial communication lines may also be set by using the **-l** command line option at test invocation.

```
13: Baud Rate for Loopback Subtests [110-73728,?]      (57600) -> ?
```

Select the baud rate to use for loopback testing. If the baud rate is not valid, a warning will be displayed and the baud rate changed to a valid value. This option may also be set using the **-b** command line option during the test invocation sequence.

```
14: Number of Iterations for Each Subtest [1-2147483647,?]
                                                          (1) -> ?
```

Enter the number of times each subtest is to be executed on the Multibus X.25 Controller. The count is passed to the controller, so the repetitions are done as quickly as possible. This is most useful for repeating a subtest many times in quick succession. This option may also be set using the **-i** command line option.

```
    ** Debug Mode Flags (bit mapped) **
0x0001: Print messages sent to COM-4
0x0002: Print messages received from COM-4
0x0004: Pause before message sent to COM-4
0x0008: Pause after message received from COM-4
0x0010: Print MBS messages sent to CCU
0x0020: Print MBS messages received from CCU
0x0040: Pause before MBS message sent to CCU
0x0080: Pause after MBS message received from CCU
0x0100: Print extra informative messages
0x0200: Don't reset COM-4 after subtest is aborted
0x0400: Don't disable SPU interrupts when done
0x0800: Simulate all MBS messages (don't send them)

15: Select Debug Mode [0x0-0xfff,?]                      (0x0) ->
```

These options allow the standard test behavior to be altered in ways that are often useful for troubleshooting. In addition, the test can be paused before and after (or both) each command (i.e., typically one controller operation) is sent to the CCU driver. These flags may also be set using the **-v** and **-d** command line options during test invocation. The first four flags (0x0001–0x0008) control printing of all messages that are sent to the Multibus X.25 Controller. The next four flags (0x0010–0x0080) independently control printing (before or after) of messages that are sent to the CCU. If the flag 0x0100 is set, verbose messages are printed just as if the **-v** options had been set from the command line. If the flag 0x0200 is set, the controller is not reset after a subtest is aborted (used for debugging). If the flag 0x0400 is set, the SPU interrupts, MBS message interrupt and CCU print interrupt, are not disabled when *dev4540* is completed. If flag 0x0800 is set, a simulation of the test is done without affecting the CCU or the controller.

NOTE

Selection of the options is achieved by entering the hexadecimal mask obtained by ORing the desired options together. For example, if the first three options are desired, enter **0x7**. If all options are desired, enter **0xfff**.

```
    ** Subtest Error Actions **
1:  Silently ignore subtest errors
2:  Pause for subtest errors
3:  Abort subtest on first error

16: Select COM-4 Subtest Error Action [1-3,?]          (2) ->
```

Enter the desired subtest error action:

- Choice 1 ignores all errors (as if they never happened). This could be useful when it is necessary to just generate constant action (for example, EMI test).
- Choice 2 passes all errors to the *dshell* for processing. Choose this option for running the test normally [default].
- Choice 3 causes the subtest to abort when the first error is seen, regardless of any *dshell* error actions specified.

```
    ** Error Start/Finish Text Options (bit mapped) **
0x0001: Enable error start text
0x0002: Enable error finish text

17: Select Error Start/Finish Message Mode [0x0-0x3,?]  (0x0) ->
```

This prompt allows a specified character string to be sent to the printer before and after (or both) an error (and its data) is displayed. Although any string up to 64 characters in length may be specified, the intended use is to selectively turn a printer on before an error is displayed and to turn a printer off after an error has been displayed. This is a paper saving feature when running *dev4540* multiple times or for long periods of time. This assumes a printer is connected to the auxiliary port on the display terminal where *dev4540* is running. It also assumes the auxiliary port can be turned on and off via an escape character sequence.

Selection of both options is achieved by entering the hexadecimal mask obtained by ORing the two options together (0x03). Control characters may be specified by using standard "C" programming style escape sequences. For example:

\033	Octal value of the ASCII escape character (0x1b)
\x1b	Same as above value but specified in hex.
\r	Carriage Return
\n	Line Feed
\t	Tab character
\b	Backspace character
\f	Form Feed character

\a	Bell ("alert") character
\v	Reverse line feed character

```
18: Error Start Character Sequence [<error start string>,?]
                                                    (\033[?5i) ->
```

Enter the string to be displayed before showing an error message. The default value is the "Enter Auto Print Mode" sequence for terminals that support VT100 terminal protocol.

Control characters may be specified by using standard "C" programming style escape sequences. For example:

\033	Octal value of the ASCII escape character (0x1b)
\x1b	Same as above value but specified in hex.
\r	Carriage Return
\n	Line Feed
\t	Tab character
\b	Backspace character
\f	Form Feed character
\a	Bell ("alert") character
\v	Reverse line feed character

```
19: Error Finish Character Sequence [<error finish string>,?]
                                                    (\033[?4i) ->
```

Enter the string to be displayed after showing an error message. The default value is the "Exit Auto Print Mode" sequence for terminals that support VT100 terminal protocol.

Control characters may be specified by using standard "C" programming style escape sequences. For example:

\033	Octal value of the ASCII escape character (0x1b)
\x1b	Same as above value but specified in hex.
\r	Carriage Return
\n	Line Feed
\t	Tab character
\b	Backspace character
\f	Form Feed character
\a	Bell ("alert") character
\v	Reverse line feed character

```
20: Enter OK, or :NN to return to question NN [OK]          (OK) ->
```

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

Multibus X.25 Controller EPROM Self-tests

The Multibus X.25 Controller contains self-diagnostic routines that are executed immediately after any reset to the controller or anytime power is applied. The controller's EPROM is always resident in memory starting at address 0xfc0000 through 0xfc3fff. The controller is reset before the first subtest and after any subtest failures. If the EPROM self-tests fail, a standard timeout error message is output by *dev4540*. When an EPROM self-test fails, the controller blinks the 8-bit error code on its single, red LED indicating the failed test. The 8-bit error code (most significant bit to least significant bit) can be identified by the sequence and duration of the blinks. Each bit of the error code occupies a constant interval of time; however, the duration of the LED blink indicates a "1" or a "0" as follows:

- A long pause (4 bit times) indicates the start of an error code
- A long blink indicates a "1"
- A short blink indicates a "0"

The error code continues blinking until the controller is reset (which causes the EPROM self-test to re-execute). The following list describes all possible EPROM error codes and their meanings (all values are binary values):

00010000 EPROM checksum wrong
00100000 EPROM system RAM (0x800–0xfff) column functionality failed
00100001 EPROM system RAM (0x800–0xfff) uniqueness test failed
00100010 EPROM system RAM (0x800–0xfff) pattern test (0x5555, first pattern) failed
00100011 EPROM system RAM (0x800–0xfff) pattern test (0xAAAA) failed
00100100 EPROM system RAM (0x800–0xfff) pattern test (0x5454) failed
00100101 EPROM system RAM (0x800–0xfff) pattern test (0xA8A8) failed
00110000 High RAM (0x01000–0x7ffff) column functionality failed
00110001 High RAM (0x01000–0x7ffff) uniqueness test failed
00110010 High RAM (0x01000–0x7ffff) pattern test (0x5555, first pattern) failed
00110011 High RAM (0x01000–0x7ffff) pattern test (0xAAAA) failed
00110100 High RAM (0x01000–0x7ffff) pattern test (0x5454) failed
00110101 High RAM (0x01000–0x7ffff) pattern test (0xA8A8) failed

EPROM Self-Test Descriptions

The following sections contain descriptions of the EPROM self-tests. In the following sections:

- System RAM refers to addresses 0x800 through 0xfff
- High RAM refers to addresses 0x01000 though 0x7ffff

Self-Test 00010000, EPROM Checksum

Self-test 00010000 verifies the EPROM checksum. The EPROM checksum is computed by summing the contents of the EPROM 32 bits at a time over the entire EPROM. If the result is non-zero, the checksum is incorrect.

Self-Test 00100000, EPROM System RAM Column Functionality

Self-test 00100000 verifies the ability to independently change each bit of local RAM. This self-test performs a walking ones test (0x0001, 0x0002, 0x0004, 0x0008, ..., 0x4000, 0x8000) and a walking zeros test (0xFFFE, 0xFFFD, 0xFFFB, 0xFFF7, ..., 0xBFFF, 0x7FFF) on the 16-bit word at location 800 in local RAM.

Self-Test 00100001, EPROM System RAM Uniqueness Test

Self-test 00100001 verifies the ability to address each system RAM location. The self-test writes an incrementing pattern (0x0001, 0x0002, 0x0003, ..., 0x0400) to system RAM. Each location is then checked to verify that it contains the correct value.

Self-Test 00100010, EPROM System RAM Pattern Test (0x5555)

Self-test 00100010 verifies the ability to check system RAM with the sequence pattern 0x5555. The self-test writes all locations with the complement of the pattern (0xAAAA), writes all locations with the pattern 0x5555, and reads and verifies all RAM locations contain the value 0x5555.

Self-Test 00100011, EPROM System RAM Pattern Test (0xAAAA)

Self-test 00100011 verifies the ability to check system RAM with the sequence pattern 0xAAAA. The self-test writes all locations with the complement of the pattern (0x5555), writes all locations with the pattern 0xAAAA, and reads and verifies all RAM locations contain the value 0xAAAA.

Self-Test 00100100, EPROM System RAM Pattern Test (0x5454)

Self-test 00100100 verifies the ability to check system RAM with the sequence pattern 0x5454. The self-test writes all locations with the complement of the pattern (0xABAB), writes all locations with the pattern 0x5454, and reads and verifies all RAM locations contain the value 0x5454.

Self-Test 00100101, EPROM System RAM Pattern Test (0xA8A8)

Self-test 00100101 verifies the ability to check system RAM with the sequence pattern 0xA8A8. The self-test writes all locations with the complement of the pattern (0x5757), writes all locations with the pattern 0xA8A8, and reads and verifies all RAM locations contain the value 0xA8A8.

Self-Test 00110000, High RAM Column Functionality

Self-test 00110000 verifies the ability to independently change each bit of local RAM. This self-test performs a walking ones test (0x0001, 0x0002, 0x0004, 0x0008, ..., 0x4000, 0x8000) and a walking zeros test (0xFFFE, 0xFFFD, 0xFFFB, 0xFFF7, ..., 0xBFFF, 0x7FFF) on the 16-bit word at location 0x1000 in local RAM.

Self-Test 00110001, High RAM Uniqueness Test

Self-test 00110001 verifies the ability to address each high RAM location. The self-test writes an incrementing pattern (0x0001, 0x0002, 0x0003, ..., 0xFFFF, 0x0001, 0x0002, ...) to high RAM. Each location is then checked to verify that it contains the correct value.

Self-Test 00110010, High RAM Pattern Test (0x5555)

Self-test 00110010 verifies the ability to check high RAM with the sequence pattern 0x5555. The self-test writes all locations with the complement of the pattern (0xAAAA), writes all locations with the pattern 0x5555, and reads and verifies all RAM locations contain the value 0x5555.

Self-Test 00110011, High RAM Pattern Test (0xAAAA)

Self-test 00110011 verifies the ability to check high RAM with the sequence pattern 0xAAAA. The self-test writes all locations with the complement of the pattern (0x5555), writes all locations with the pattern 0xAAAA, and reads and verifies all RAM locations contain the value 0xAAAA.

Self-Test 00110100, High RAM Pattern Test (0x5454)

Self-test 00110100 verifies the ability to check high RAM with the sequence pattern 0x5454. The self-test writes all locations with the complement of the pattern (0xABAB), writes all locations with the pattern 0x5454, and reads and verifies all RAM locations contain the value 0x5454.

Self-Test 00110101, High RAM Pattern Test (0xA8A8)

Self-test 00110101 verifies the ability to check high RAM with the sequence pattern 0xA8A8. The self-test writes all locations with the complement of the pattern (0x5757), writes all locations with the pattern 0xA8A8, and reads and verifies all RAM locations contain the value 0xA8A8.

Class Descriptions

The *dev4540* test contains the four classes of subtests listed in the following table:

Table dev4540–8, *dev4540* Test Classes

CLASS	DESCRIPTION
1	Multibus X.25 EPROM-Based Controller Tests
2	Multibus X.25 Internal Loopback Tests
3	Multibus X.25 External Connection Tests (External Transmit Clock)
4	Multibus X.25 External Connection Tests (Internal Transmit Clock)

All subtests contained in *dev4540* are loopable under the *dshell*.

Class 1 Subtests

Class 1 subtests consist of basic controller tests involving EPROM, parity, interrupt, and RAM. Class 1 subtests test only the Multibus X.25 Controller; no Serial Communications Interface (SCI) modules are required. Class 1 subtests verify:

- The ability to communicate with the Multibus Input/Output Processor (MIOP), Multibus Control Unit (MBCU), and the Multibus X.25 Controller
- The ability of the Multibus X.25 Controller to interrupt the MIOP
- The EPROM checksum is correct
- The Multibus X.25 Controller RAM is fully functional:
  - Each RAM location is unique (no aliasing)
  - The RAM is pattern tested for data correctness
- Parity checking logic is fully functional

Table dev4540–9, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
100	Multibus X.25 Basic Controller Test	00:40[1]
101	Multibus X.25 RAM Pattern Test	00:35[2]
102	Multibus X.25 RAM Parity Test	00:01

[1] Time varies depending on whether or not the controller must complete its power-on self-check.
[2] Time varies depending on the number of patterns input for testing.

Subtest 100, Multibus X.25 Basic Controller Test

Subtest 100 verifies the EPROM checksum and tests RAM locations 0x01000 through 0x7FFFF. The EPROM checksum is computed by summing the contents of the EPROM 32 bits at a time over the entire EPROM. If the result is non-zero, the checksum is incorrect.

The RAM test consists of the following parts (in order of execution):

- Column test: verify ability to independently change each bit
- Uniqueness test: verify ability to address each RAM location
- Pattern test: check RAM with the sequence of patterns 0x5555, 0xAAAA, 0x5454, 0xA8A8.

NOTE

This subtest duplicates tests executed in the EPROM power-on self-test code. This means any non-intermittent problems in these areas are likely to cause self-test failures (indicated with the red LED on the controller). For detailed descriptions of these subtest routines, refer to the "EPROM Self-Test Descriptions" section in this chapter.

Subtest 101, Multibus X.25 RAM Pattern Test

Subtest 101 verifies RAM locations 0x01000 through 0x7FFFF with a pattern test, using up to 32 patterns specified by the user. The default patterns are shown in the following table:

Table dev4540–10, Subtest 101 Default Test Patterns

Description	Hexadecimal Pattern
All zeros	00000000
All ones	FFFFFFFF
Individual 1 bits	01010101, 02020202, 04040404, 08080808, 10101010, 20202020, 40404040, 80808080
Individual 0 bits	FEFEFEFE, FDFDFDFD, FBFBFBFB, F7F7F7F7, EFEFEFEF, DFDFDFDF, BFBFBFBF, 7F7F7F7F
Alternate 1 and 0	55555555, AAAAAAAA
Two 1's and a 0	DB6DB6DB, B6DB6DB6, 6DB6DB6D
Two 0's and a 1	24924924, 49249249, 92492492
Two 1's and two 0's	CCCCCCCC, 99999999, 33333333, 66666666

Subtest 102, Multibus X.25 RAM Parity Test

Subtest 102 verifies correct operation of the Multibus X.25 Controller RAM parity checking. It verifies both even and odd parity, including both correct and incorrect parity. The patterns used to check the parity operations are shown in the following table:

Table dev4540–11, Subtest 102 Parity Check Patterns

Description	Hexadecimal Pattern
All zeros	00
All ones	FF
Individual 1 bits	01, 02, 04, 08, 10, 20, 40, 80
Individual 0 bits	FE, FD, FB, F7, EF, DF, BF, 7F
Alternate 1 and 0	55, AA
Two 1's and a 0	DB, B6, 6D
Two 0's and a 1	24, 49, 92
Two 1's and two 0's	CC, 99, 33, 66

Class 2 Subtest

The class 2 subtest verifies only the Multibus X.25 Controller. No Serial Communications Interface (SCI) modules are required. The class 2 subtest performs a system check that tests the following functional units:

- Serial Communications Controllers (SCC) in loopback mode
- Direct Memory Access (DMA) controllers
- Interrupt generation and arbitration logic

The system check is executed using both local (Multibus X.25 Controller) memory and main memory mapped via Multibus as the source of DMA data to the SCC.

Table dev4540–12, Class 2 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
200	Multibus X.25 System Test (Internal Loopback)	00:12[1]

[1] Time varies depending on the selected baud rate.

Subtest 200, Multibus X.25 System Test (Internal Loopback)

Subtest 200 tests the DMA controllers, SCC controllers, interrupt controller, and bus interface. The subtest is designed to use the components together as a system to check for interactions between parts as well as testing individual parts. The subtest executes with the SCC in local loopback mode. This test does not require any external connections; the Multibus X.25 Controller is all that is necessary.

Subtest 200 is designed to use DMA to send data through the SCC, loop the data back to the SCC (in local loopback mode), and read the data from the SCC with DMA. Various SCC and

DMA interrupts are enabled and checked, including DMA completion interrupts.

The subtest logic is:

- Fill source buffer with the incrementing pattern (00, 01, 02, ..., FE, FF, 00, ...)
- Reset all SCC channels
- Initialize selected SCC channels for transfer in SDLC mode
- Initialize DMA channels corresponding to the SCC channels
- Set up a timeout based on baud rate and transfer size
- Start the transfer
- Wait until transfer completes or timeout expires
- Verify that received data pattern matches source data

This subtest logic is executed three times. The first execution uses a small buffer (128 bytes) in controller local memory as the source buffer. The second execution uses a large buffer (8 Kbytes) in controller local memory as the source buffer. The third execution uses a buffer (one page – 4,096 bytes) in IOP local memory accessed via the cache controller (mapped to Multibus memory).

Class 3 Subtests

Class 3 subtests verify communication through the Serial Communications Interface (SCI) modules. Subtest 301 requires the use of an external loopback jumper (refer to the "Prerequisites and Required Equipment" section in this chapter for the CONVEX part number). The subtests run the same system check used by class 2 except that subtest 301 sends the data through the SCI modules and subtest 300 uses the SCC loopback mode with the clock supplied by the modem.

For any given system configuration, only subtests from either class 3 or class 4 are executed. Class 3 is executed for the standard configuration with the Transmit Clock signal supplied by the external device (typically a modem).

Class 3 subtests are different variations of a system test that tests the DMA controllers, SCC controllers, interrupt controller, and bus interface. The subtests use the components together as a system to check for interactions between parts as well as testing individual parts.

The subtests use DMA to send data through the SCC, loop the data back to the SCC (depending on which subtest), and read the data from the SCC with DMA. Various SCC and DMA interrupts are enabled and checked, including DMA completion interrupts.

The logic of the subtests is:

- Fill source buffer with the incrementing pattern (00, 01, 02, ..., FE, FF, 00, ...)
- Reset all SCC channels
- Initialize selected SCC channels for transfer in SDLC mode
- Initialize DMA channels corresponding to the SCC channels
- Set up a timeout based on baud rate and transfer size
- Wait for Data Carrier Detect (DCD) to be active for selected SCC channels
- Start the transfer
- Wait until transfer completes or timeout expires
- Verify that received data pattern matches source data

This subtest logic is executed three times. The first execution uses a small buffer (128 bytes) in controller local memory as the source buffer. The second execution uses a large buffer (8 Kbytes) in controller local memory as the source buffer. The third execution uses a buffer (one page – 4,096 bytes) in IOP local memory accessed via the cache controller (mapped to Multibus memory). The following table lists all class 3 subtests, their descriptions, and the time required to execute them:

> **NOTE**
>
> Subtest 301 is only applicable for versions of *dev4540* with build dates later than July 19, 1989. Earlier versions of this diagnostic do not contain subtest 301 and subtest 300 has different functionality. Refer to subtest 300's description for details.

Table dev4540–13, Class 3 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
300	Multibus X.25 System Test (External Clock Source, DCE Tx Clock)	00:12[1]
301	Multibus X.25 System Test (External Loopback, DCE Tx Clock)	00:12[1]

[1] Time varies depending on the selected baud rate.

Subtest 300, Multibus X.25 System Test (External Clock source, DCE Tx Clock)

Subtest 300 is for use with Multibus X.25 Controllers and SCI modules that are jumpered to use the transmit clock from the modem as the Tx clock source (the standard configuration). Subtest 300 tests the clocks from the modem to ensure that the jumpers are set up correctly on the controller, the SCI module, and the modem. The transmit and receive clocks from the modem are used, but the data is looped back through the SCC internal loopback option. No external loopback connectors are necessary to execute this subtest, although a modem must be connected to provide the transmit and receive clock signals.

> **NOTE**
>
> This description of Subtest 300 applies to versions of *dev4540* built after July 19, 1989. The version of *dev4540* can be determined with the **-V** command line option issued during test invocation. In earlier versions of the diagnostic, subtest 300 performed the same functionality as subtest 401 with external connect option set to 0x1.

Subtest 301, Multibus X.25 System Test (External Loopback, DCE Tx Clock)

Subtest 301 is for use with the Multibus X.25 Controller and SCI modules which are jumpered to use the transmit clock from the modem as the Tx clock source (the standard configuration). Subtest 301 tests the data paths from the Multibus X.25 Controller to the external panel and back to the controller. The transmit and receive clocks used depend on whether or not a modem is present. If a modem is present, the clocks from the modem are used; if no modem is present, the SCC's baud rate generator is used as both the transmit and receive clocks. A loopback cable (refer to the "Prerequisites and Required Equipment" section in this chapter for the CONVEX part number) must be installed for this subtest to execute correctly.

> **NOTE**
>
> This description of Subtest 301 applies to versions of *dev4540* built after July 19, 1989. The version of *dev4540* can be determined with the **-V** command line option. This subtest does not exist in earlier versions of the diagnostic.

Class 4 Subtests

Class 4 subtests verify communication through the Serial Communications Interface (SCI) modules. Subtest 401 requires the use of an external loopback jumper (refer to the "Prerequisites and Required Equipment" section in this chapter for the CONVEX part number). The subtests run the same system check used by class 2 except that subtest 401 sends the data through the SCI modules and subtest 400 uses the SCC loopback mode with the clock supplied by the modem.

Class 4 subtests are different variations of a system test that tests the DMA controllers, SCC controllers, interrupt controller, and bus interface. The subtests use the components together as a system to check for interactions between parts as well as testing individual parts.

For any given system configuration, only subtests from either class 3 or class 4 are executed. Class 4 is executed for alternate configurations with the Transmit Clock signal supplied by the Multibus X.25 Controller.

The subtests use DMA to send data through the SCC, loop the data back to the SCC (depending on which subtest), and read the data from the SCC with DMA. Various SCC and DMA interrupts are enabled and checked, including DMA completion interrupts.

The logic of the subtests is:

- Fill source buffer with the incrementing pattern (00, 01, 02, ..., FE, FF, 00, ...)
- Reset all SCC channels
- Initialize selected SCC channels for transfer in SDLC mode
- Initialize DMA channels corresponding to the SCC channels
- Set up a timeout based on baud rate and transfer size
- Wait for Data Carrier Detect (DCD) to be active for selected SCC channels
- Start the transfer
- Wait until transfer completes or timeout expires
- Verify that received data pattern matches source data

Each subtest executes this subtest logic three times. The first execution uses a small buffer (128 bytes) in controller local memory as the source buffer. The second execution uses a large buffer (8 Kbytes) in controller local memory as the source buffer. The third execution uses a buffer (one page – 4,096 bytes) in IOP local memory accessed via the cache controller (mapped to Multibus memory).

> **NOTE**
>
> Subtest 401 is only applicable for versions of *dev4540* with build dates later than July 19, 1989. Earlier versions of this diagnostic do not contain subtest 401 and have different functionality in subtest 400. Refer to subtest 400's description for details.

Table dev4540–14, Class 4 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
400	Multibus X.25 System Test (External Clock source, DTE Tx Clock)	00:12
401	Multibus X.25 System Test (External Loopback, DTE Tx Clock)	00:12

Subtest 400, Multibus X.25 System Test (External Clock source, DTE Tx Clock)

Subtests 400 and 401 are for use with the Multibus X.25 Controller and SCI modules that are jumpered to use the receive clock from the modem as the Tx clock source. This is a nonstandard configuration that allows more thorough diagnostic testing.

Subtest 400 tests the clocks from the modem to ensure that the jumpers are set up correctly on the controller, the SCI module, and the modem. The receive clock from the modem is used as both the transmit and receive clocks, but the data is looped back through the SCC internal loopback option. No external loopback connectors are necessary to execute this subtest, although a modem must be connected to provide the receive clock signal.

NOTE

This description of Subtest 400 applies to versions of *dev4540* built after July 19, 1989. The version of *dev4540* can be determined with the **-V** command line option issued during test invocation. In earlier versions of the diagnostic, subtest 400 performed the same functionality as subtest 401 with external connect option set to 0x5.

Subtest 401, Multibus X.25 System Test (External Loopback, DTE Tx Clock)

Subtest 401 is for use with the Multibus X.25 Controller and SCI modules which are jumpered to use the receive clock from the modem as the Tx clock source. This is a nonstandard configuration which allows more thorough diagnostic testing.

Subtest 401 tests the data paths from the Multibus X.25 Controller to the external panel and back to the controller. The controller always sends a transmit clock to the SCI module as the external transmit clock. If a modem is present, the receive clock from the modem is used as the transmit clock; if no modem is present, the baud rate generator is used to generate a transmit clock. The receive clock is always taken from the external connection. If a modem is present, the receive clock is from the modem. If no modem is present, the loopback cable connects the external transmit clock to the receive clock, so the receive clock is an echo of the transmit clock. A loopback cable must be installed for this subtest to execute correctly (refer to the "Prerequisites and Required Equipment" section in this chapter for the CONVEX part number).

NOTE

Subtest 401 is only applicable for versions of *dev4540* with build dates later than July 19, 1989. Earlier versions of this diagnostic do not contain subtest 401 and have different functionality in subtest 400. Refer to subtest 400's description for details.

Error Messages

There are three basic types of error messages associated with this diagnostic:

- Error messages associated with the diagnostic's start-up
- Error messages associated with the execution of the diagnostic's subtests (related with system errors)
- Error messages associated with the execution of the diagnostic's subtests (related with subtest errors)

Start-Up Error Messages

The first type of error message is output after start-up errors (i.e., before the first subtest is executed). These messages usually do not contain header or footer information. The following error messages may occur during the start-up sequence of the diagnostic:

```
COM-4 68010 Bus Error Exception  (0x02)

COM-4 68010 Address Error Exception  (0x03)

COM-4 68010 Parity Error Exception  (0x1E)

Unable to initialize processor queues  (0x01)

Unable to initialize CCU  (0x04)

Unable to configure SCI-001 driver  (0x05)

Unable to probe SCI-001 driver  (0x06)

File is not in b.out format  (0x07)

Timeout waiting for CCU driver reply  (0x08)

MBS error occurred  (0x09)

File not found  (0x0A)

Invalid command  (0x10)

COM-4 not initialized  (0x11)

Timeout waiting for COM-4 reply  (0x12)

COM-4 is owned by another process  (0x13)

Unable to allocate CCU windows for message  (0x14)

No message buffers available for message  (0x15)

Unable to reset board (bad CSR?)  (0x16)

Unable to write to send interrupt  (0x17)

Unable to write to clear interrupt  (0x18)
```

```
COM-4 did not go idle/not stopped for debug  (0x19)

COM-4 did not respond to FL_READY  (0x1A)

COM-4 did not interrupt when done  (0x1B)

Unable to allocate main memory  (0x1C)

Pending message flushed by IOP  (0x1D)

Write to COM-4 memory failed  (0x1F)

Error setting up test  (0x20)

COM-4 has wrong status  (0x21)
```

General Error Messages

The second type of *dev4540* error message can occur at anytime during the execution of the diagnostic. These error messages are usually non-subtest related errors that occur while a subtest is executing. Each error message contains a standard header and footer. The message, placed between the header and footer, will consist of one or more of the error messages listed in the first type of error messages (start-up error messages). The following figure contains an example of the standard header message:

Figure dev4540–5, Standard Header for Error Messages

```
*****  Sun Jul 16 15:04:10 1989  *****
Test:    dev4540.t  1.1    Class: 1    Subtest: 100 1.2   Count: 1    Error: 0
Failed:  Multibus X.25 Basic Controller Test
```

The following figure contains an example of a standard footer that is printed after the standard header and error message:

Figure dev4540–6, Standard Footer for Error Messages

```
Test 'dev4540.t' failed
Elapsed time:   0:00:03
```

Subtest Error Messages

The third type of error messages are errors reported by an executing subtest (i.e., subtest failures). Each error message contains a standard header and footer that are included with the message. Also, the error message contains the following information:

- Iteration—lists which iteration of the subtest was being executed at the time of the failure
- State—describes the current program status, usually "Paused for error."
- Reason(s)—describes the error condition and usually contains actual and expected values

The following list contains all possible reasons that could be listed in the error message:

```
Reason(s):      Unexpected odd parity at address 0xXXXXXXX
                Expected: ddd  Actual: ddd

Reason(s):      Unexpected even parity at address 0xXXXXXXX
                Expected: ddd  Actual: ddd

Reason(s):      Didn't get expected odd parity at address 0xXXXXXXX
                Expected: ddd  Actual: ddd

Reason(s):      Didn't get expected even parity at address 0xXXXXXXX
                Expected: ddd  Actual: ddd

Reason(s):      Serial Communications Controller error
                Unexpected SCC interrupt, line d
                Didn't receive SCC interrupt, line d
                Transmit underrun, line d
                Abort received, line d
                CRC error or Receive overrun, line d

Reason(s):      Timeout waiting for DMA to finish
                Unexpected interrupt, DMA channel d (line d transmit)
                Unexpected interrupt, DMA channel d (line d receive)
                Didn't receive interrupt, DMA channel d (line d transmit)
                Didn't receive interrupt, DMA channel d (line d receive)

Reason(s):      Data verify failed at offset 0xXXXXXXX on line d
                Expected: 0xXXXX  Actual: 0xXXXX

Reason(s):      Controller EPROM checksum error (checksum is 0xXXXXXXXXX)

Reason(s):      RAM check failed at 0xXXXXXX
                Expected: 0xXXXX  Actual: 0xXXXX  (subtest 100)
                Expected: 0xXXXXXXXX  Actual: 0xXXXXXXXX  (subtest 101)
                Expected: 0xXX  Actual: 0xXX  (subtest 102)

Reason(s):      Timeout waiting for DCD to become active
                DCD not active, line d

Reason(s):      Invalid Diagnostic command

Reason(s):      Invalid subtest number

Reason(s):      Subtest failed
```

```
Reason(s):      Subtest aborted

Reason(s):      A test is already running

Reason(s):      No test is currently running

Reason(s):      No test is waiting to continue

Reason(s):      COM-4 RAM test program not running
```

Examples of the standard header and footer messages are shown in the description of the General Error error messages.

dev4600

Multibus Emulator Controller Test

Overview

The *dev4600* test checks the IKON DR-11W Emulator model 10077. Certain operating modes and signals are not tested. Items not tested include byte-mode I/O, and read-after-write DMA mode, and certain signals not used for interprocessor link. In addition, the following external signals are not tested:

Table dev4600–1, Untested External Signals

DIRECTION	NAME
Output	READY H GO H END CYCLE H

Also, the following external signals are only partially tested:

Table dev4600–2, Partially Tested Signals

DIRECTION	NAME	DESCRIPTION
Output	BUSY H	When switched for high assertion
	INIT H	Assertion not tested
Input	CO CNTL H	Read-modify-write and write bytes not tested
	CYCLE RQ B H	Request cycle input B not tested
	WC INC ENB H	Suppress word count increment not tested
	BA INC ENB H	Suppress word address increment not tested
	A00 H	Byte write select not tested

Prerequisites and Required Equipment

The *dev4600* test requires a functional IKON controller model 10077. Class 3 subtests require the use of a second functional DR-11W mounted in the same Multibus.

> **NOTE**
>
> For most subtests, Classes 1 and 3, two normal DR-11W data cables, CONVEX part number 604-100004-002, are required. However, to execute the Class 2 Subtest, a special loopback cable, CONVEX part number 604-100004-001, is required.

The following table lists the required hardware depending on the type of machine under test.

Table dev4600–3, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
IOP	IOP
MBCU	MBCU
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Test Invocation

The *dev4600* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev4600* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev4600–1, Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev4600 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev4600** executes all *dev4600* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual. The [+>*filename*] option allows the test results to be appended to *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev4600–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev4600 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev4600–4, Getting Help During Test Parameter Entry

Character	Description
?	Displays this help menu
h	Provides help for a specific prompt
i	Displays the */ioconfig* file

After the desired help information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev4600–3, Test Parameter Menu

```
                    ENTER TEST PARAMETERS

          []      Encloses allowed input ranges or values
          ()      Encloses the default value
          ^       Returns to the previous prompt
          :nn     Returns to the prompt # nn
          :       Returns to the first unsatisfied prompt
          :?      Reviews previous entries
          ?       Provides additional help for each question

           PERIPHERAL CONFIGURATION DATA
    CCU   Chassis  Type    CSR   Int Unit Type
   ------- ------- -------- ----- --- ---- --------

Device 0 = user defined configuration

 1: Device Under Test Selection [0,?]                    (0) ->
 2: Controller Under Test IOP [3-7][1]                   () ->
 3: Controller Under Test Multibus Chassis [0-3]         () ->
 4: Controller Under Test Offset in Multibus [0x0-0xfff] () ->
 5: Controller Under Test Interrupt Number [0-7]         () ->

             PERIPHERAL CONFIGURATION DATA
    CCU   Chassis Type    CSR   Int Unit Type
   ------- ------- -------- ----- --- ---- --------

Device 0 = user defined configuration

 6: Loopback Device Selection [0,?]                      (0) ->
 7: Loopback Controller Offset in Multibus [0x0-0xfff]   () ->
 8: Loopback Controller Interrupt Number [0-7]           () ->
 9: Test Instructions [y,n]                              (n) ->
10: Enter OK, or :NN to return to question NN [OK]       (OK) ->
```

[1] The possible selections for this prompt will change depending on machine architecture.

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

A description of the meaning of each prompt follows:

```
Device Under Test Selection [0, ?]                    (0) ->
```

This prompt selects the device for testing from the system configuration file. The number entered indicates the device to be tested. If **0** is entered, prompts 2-5 are displayed for manually specifying the device test parameters. Any valid value other than **0** will *not* display prompts 2-5 and skips to prompt 6, **Loopback Device Selection**.

```
Controller Under Test IOP [3-7]                       () ->
```

This prompt begins the queries for user-defined devices; additional prompts are displayed requesting hardware configuration information. Enter the CCU slot number of the IOP for the corresponding controller under test.

```
Controller Under Test Multibus Chassis [0-3]          () ->
```

Enter the Multibus chassis number that the controller under test resides in.

```
Controller Under Test Offset in Multibus [0x0-0xfff]  () ->
```

Enter the low-order 12 bits of the controller's address within the Multibus.

```
Controller Under Test Interrupt Number [0-7]          () ->
```

Enter the interrupt level of the controller within the Multibus.

```
Loopback Device Selection [0, ?]                      (0) ->
```

If Class 3 subtests are to be executed, the specification of the second DR-11W must be entered. This prompt is only displayed when a Class 3 subtest is to be executed. The prompt allows for selection of a known good device (used for loopback testing of the device under test) from the system configuration file. The number entered for the prompt indicates the device to be tested. If **0** is entered for a device number, then prompts 7-8 are displayed. Any valid value other than 0 will *not* display prompts 7-8 and skips to prompt 9, **Test Instructions**. If **0** is entered, prompts 7-8 allow for manually specifying the loopback device parameters.

```
Loopback Controller Offset in Multibus [0x0-0xfff]    () ->
```

Enter the low-order 12 bits of the loopback controller's address within the Multibus.

```
Loopback Controller Interrupt Number [0-7]            () ->
```

Enter the interrupt level of the loopback controller within the Multibus.

```
Test Instructions [y,n]                               (n) ->
```

If **y** is entered, a page of information about the required test cables for loopback and parity testing is displayed.

```
Enter OK, or :NN to return to question NN [OK]        (OK) ->
```

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure dev4600–4, Sample Test Parameter Summary

```
                TEST PARAMETER SUMMARY

Controller Under Test IOP                          : 3
Controller Under Test Multibus Chassis             : 0
Controller Under Test Offset in Multibus           : 0x0
Controller Under Test Interrupt Number             : 0
Loopback Controller Offset in Multibus             : 0x100
Loopback Controller Interrupt Number               : 1
Test Instructions                                  : n
Enter OK, or :NN to return to question NN          : OK
```

If standard output is directed to a disk file, the test parameter summary is also directed to the disk file.

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The IOP is booted and loaded
- A driver on the IOP is started
- IOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev4600* test contains the following three classes of subtests as shown in the following table:

Table dev4600–5, *dev4600* Test Classes

CLASS	DESCRIPTION
1	Loopback tests
2	Parity-loopback test
3	Dual Emulator DMA tests

Class 1 Subtests

Class 1 subtests verify the basic functionality of the controller. The subtests include board reset and loopback tests. Class 1 subtests are listed in the following table:

Table dev4600–6, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
100	Reset Capability	0:01
101	Programmed I/O Loopback	0:14
102	FCNx, STTx Status	0:01
103	Attention Signal/Flag	0:01
104	DMA Preparatory	2:00
105	DMA Abort Via Attention and Reset	0:02
106	Interrupt	0:02
107	DMA Output Loopback	1:17
108	DMA Input Loopback	0:11

Subtest 100, Reset Capability

Subtest 100 verifies that the controller resets properly by checking the status register for the correct value. The controller must generate no interrupt.

Subtest 101, Programmed I/O Loopback

Subtest 101 assures that programmed I/O works properly by checking the data paths and parity generation/check capability. The parity check is not complete until Subtest 200 is also successfully passed.

Subtest 102, FCNx, STTx Status

Subtest 102 checks the user-function codes and status flags.

Subtest 103, Attention Signal/Flag

Subtest 103 checks the attention signal status and attention flag status. This subtest also tests the commands for resetting the attention flag and checks for proper function on reset.

Subtest 104, DMA Preparatory

Subtest 104 checks for proper board status during the stages of DMA initiation. This subtest also verifies DMA direction.

Subtest 105, DMA Abort Via Attention and Reset

Subtest 105 checks that DMA operations can be properly aborted via the attention input signal or board reset.

Subtest 106, Interrupt

Subtest 106 tests the IKON capability to generate an interrupt on attention assertion or DMA completion. In addition, this subtest tests the capability for board reset to clear this interrupt.

Subtest 107, DMA Output Loopback

Subtest 107 performs DMA output to the output data register. This subtest checks the last value in each DMA buffer by reading the value from the input data register after the DMA block is finished. Only the last word in the block can be checked.

Word patterns are tested by passing buffers ending with 0x*nnnn*, where *n* varies from 0 to 0xf. Each 100-word buffer is filled with random data (except for the last entry), generated using *rand*() with a seed value of 137 plus 0x*nnnn*.

In addition, the subtest tests a range of buffer sizes; each buffer contains random data patterns. The random values are generated using *rand* () with a seed value of 137 plus the buffer size. The last value in each buffer, which is described in the following table, is complemented for each buffer size tested.

This subtest tests the following DMA buffer sizes (hex values):

Table dev4600–7, DMA Buffers Sizes Tested

INITIAL SIZE	SIZE INCREMENT	SIZE LIMIT	ALTERNATING FINAL VALUE
1	1	10	[~]AAAA
11	11	100	[~]CCCC
101	111	1000	[~]EEEE
1001	1111	10000	[~]1111
FFFE	1	10000	[~]0000

Subtest 108, DMA Input Loopback

Subtest 108 performs Direct Memory Access (DMA) input of word patterns from the input data register. The subtest primes the input data register by writing to the output data register and through the loopback cable. The same fixed value is transferred into all words of the input buffer since the input data register is not changed while DMA is in progress.

Word patterns are tested by priming the input data register to 0x*nnnn*, where *n* varies from 0 to 0xf. The subtest reads in 100-word blocks.

Both this subtest and Subtest 107 test the same range of DMA buffer sizes; refer to Subtest 107 for a listing of buffer sizes tested.

Class 2 Subtest

The Class 2 subtest verifies correct operation of the parity circuits.

> **NOTE**
>
> A special loopback cable, CONVEX part number 604-100004-001, is required to execute this test.

The Class 2 subtest is listed in the following table:

Table dev4600–8, Class 2 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
200	Data Parity	0:16

Subtest 200, Data Parity

Subtest 200, which complements Subtest 101, checks the parity-checking circuitry. This subtest uses data patterns of known parity to verify that the parity checking circuits pass good parity and also detect bad parity.

> **NOTE**
>
> A special loopback cable is required, CONVEX part number 604-100004-001, to execute this subtest. The cable allows input parity to be driven from a known good data bit (checked in Subtest 101).

Class 3 Subtests

Class 3 subtests verify correct operation of the DMA circuits by exchanging data between two emulators. Class 3 subtests are listed in the following table:

Table dev4600–9, Class 3 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
300	DMA Output	1:36
301	DMA Input	1:37

Subtest 300, DMA Output

Subtest 300 uses a second DR-11W Emulator to receive DMA output data from the DR-11W Emulator under test to test a data block containing all possible word patterns. In addition, this subtest tests blocks of varying sizes containing random patterns. Random numbers are generated using a seed value of 137 plus the buffer size.

This subtest tests the following DMA buffer sizes (hex values):

Table dev4600–10, DMA Buffer Sizes Tested

INITIAL SIZE	SIZE INCREMENT	SIZE LIMIT
1	1	10
11	11	100
101	111	1000
1001	1111	10000
FFFE	1	10000

Subtest 301, DMA Input

Subtest 301 uses a second DR-11W Emulator to transmit DMA input data to the DR-11W Emulator under test to test a data block containing all possible word patterns. In addition, this subtest tests blocks of varying sizes containing random patterns, which are generated using *rand*() with a seed value of 137 plus the buffer size. Both this subtest and Subtest 300 test DMA buffers of the same size; refer to Subtest 300 for a listing of buffer sizes tested.

Error Messages

Datum: [**expected** *0xnn*] [**actual** *0xnn*] [**offset** *0xnn*]

This logs a data byte, including expected value, in case of error. The offset, if given, specifies an offset in a data buffer.

Erroneous interrupt
IKON status: expected *0xnnn*, **actual** *0xnn*, **differences:**
{Interpretation}

An interrupt has occurred. Refer to "IKON status" for interpretation detail.

Exception for iop d from recv_iop
{error message detail}

An error has occurred using the SPU/IOP interface to wait for a signal from the IOP that the command is finished. Refer to "Exception from setup_iop" for message detail.

Exception from load_iop
{error message detail}

An error has occurred while bootstrapping the IOP. Make sure that the IOP program image file *dev4600.x00* is available and readable. It must reside either in the current directory or */mnt/test*. Refer to "Exception from setup_iop" for message detail.

Exception from send_iop (n)
{error message detail}

An error has occurred using the SPU/IOP interface to signal the IOP that a command is ready. Refer to "Exception from setup_iop" for message detail.

Exception from setup_iop
{error message detail}

An error occurred when preparing to access the IOP. When this error occurs, the message detail may be the following:

Table dev4600–11, IOP Access Error Messages

TEXT	MEANING
HARD ERROR	Hardware error
IOP BUS ERROR	Controller address error
IOP CACHE ERROR	IOP hardware error
IOP PBUS ERROR	IOP hardware error
MMIO ERROR	Main memory error
MULTIBUS ERROR	Hardware error
TIMEOUT	Possible hardware error

Exception from start_iop
{error message detail}

An error has occurred while starting the IOP. Refer to "Exception from setup_iop" for message detail.

Exception in mmalloc_init. Is main memory initialized?

There is a problem accessing main memory. Assure that main memory is present; initialize, if necessary, using *mminit*. If problems persist, consult the Technical Assistance Center.

Function status: message
{UNIX error message if applicable}

There is a problem in IOP processing. The following messages may be displayed:

Table dev4600–12, IOP Processing Error Messages

TEXT	MEANING
UNIX ERROR	Error specified in message
SUBSYSTEM WON'T GO READY	Hardware problem

IKON status 0xnn **means:**
{interpretation}

This is the IKON status word. The following interpretation may be displayed:

Figure dev4600–5, Interpreted Status Word Error Messages

```
DMAF:  DMA END-RANGE FLAG [NOT] SET
ATTF:  ATTENTION FLAG [NOT] SET
ATTN:  ATTENTION INPUT [NOT] SET
PERR:  PARITY FLAG [NOT] SET
STTA:  STATUS A INPUT [NOT] SET
STTB:  STATUS B INPUT [NOT] SET
STTC:  STATUS C INPUT [NOT] SET
REDY:  IKON [NOT] READY
IENB:  IKON INTERRUPTS [NOT] ENABLED
FCN3:  FCN3 LATCH [NOT] SET
FCN2:  FCN2 LATCH [NOT] SET
FCN1:  FCN1 LATCH [NOT] SET
```

IKON status: expected 0xnn, **actual** 0xnn, **differences:**
{interpretation}

An unexpected status code was obtained. The differences between the actual code and what was desired are interpreted (refer to previous error message).

Main memory allocation error

There is a problem allocating main memory. Be sure that main memory is present and initialized. If problems persist, consult the Technical Assistance Center.

Missing interrupt

IKON expected interrupt code *0xnn*
{Interpretation}

An interrupt, which should have occurred, did not occur. Refer to "IKON status" for interpretation detail.

Spurious interrupt error: *dd* **expected,** *dd* **actual**

The count of spurious interrupts was not as expected. Spurious interrupts are those which are redundant.

Unexpected interrupt
IKON actual interrupt code 0xnn
{interpretation}

An interrupt that was not expected occurred. Refer to "IKON status" for interpretation detail.

dev5130

VMEbus SMD/ESDI Disk Test and Formatter

Overview

Test *dev5130* is a multi-purpose disk test which allows the user to do the following:

- Verify Interphase 4200 VMEbus/Storage Module Device (V/SMD) and Interphase 4201 VMEbus/Enhanced Small Device Interface (V/ESDI) disk controllers and attached drives operate properly.
- Format or reformat up to 12 drives at one time.
- Verify previously formatted drives.
- Perform disk maintenance such as slipping of bad sectors and mapping bad tracks to alternate tracks. All maintenance operations can be performed nondestructively so user data can be retained.

CAUTION

Some subtests in *dev5130* are data destructive.

WARNING

CONVEX UNIX cannot be running concurrently with the *dev5130* test.

This test description is intended as a reference for users who have a good understanding of disk architecture and basic controller operations and want a tool that will allow them to track down and fix often difficult to locate problems with disks. For the casual user, in other words, the person who wants to format a disk now and then or slip a defective sector or verify a disk by reading all the usable parts, the user should refer to the section "Examples of Typical Usage of This Test" within this test description. It is suggested that the Table of Contents be used as an outline for finding information within this test.

The *dev5130* test is divided into two code bodies designated *dev5130.t* and *dev5130.x00*. The code bodies *dev5130.t* and *dev5130.x00* refer to Service Processor Unit (SPU) and VIOP resident code, respectively. The first body of code *dev5130.t* executes under the *dshell* from SPU UNIX. The primary function of this code body is to interface the user to the test and to control the testing sequence. This interface software consists of user prompts and error message printouts for all subtests except Subtest 300, Format Setup and Subtest 400, Interactive Test. The user prompts depend on the *dshell* extension routine *read_parm* for user inputs. The use of this routine allows the user interface of *dev5130.t* to be directly compatible with the other peripheral test programs.

Subtests 300 and 400 are interactive with their own prompts and set of commands including help commands.

The second body of code is *dev5130.x00* and executes under the Event Governed Operating System (EGOS). This body of code contains the command processing software used to test the controller(s) and SMD devices. The code communicates to the Service Processor via the Message-Based Subsystem (MBS) and through main memory.

Prerequisites and Required Equipment

The SMD 4200 or ESDI 4201 controller must be configured for use. This is accomplished by changing jumpers on the board. Only changes to the VMEbus address of the controller are supported by this test. All other jumpers must be in a predefined configuration. All jumpers except the bus request block and address jumpers should be set properly by Interphase.

The configuration options and the CONVEX configuration are defined in the following table:

Table dev5130–1, 4200 Controller Jumper Configurations

CONFIGURATION OPTION	POSSIBLE CONFIGURATIONS	CONVEX CONFIGURATIONS
Address Modifier	0x29; 0x2D	0x2D
Base Address	0x0000,0x0200,...,0xFE00	Any are possible
Bus Request Priority	0-3	3

All other jumpers are for factory use only and should not be changed.

The test requires the system configuration in one of the next two table depending on the type of machine under test.

Table dev5130–2, Hardware Requirements (C1, C120)

ITEM	MINIMUM	MAXIMUM
Interphase SMD 4200/ESDI 4201 controller	1	12
SMD device	1	12
Input/output processor (VIOP)	1	5
Multibus card cage	1	10 (2/IOP)
Service processor unit (SPU)	1	1
VMEbus control unit (VBCU)	1	12
Memory control unit (MCU)	1	1
Memory array unit (MAU)	4MB	System limit

Table dev5130–3, Hardware Requirements (C200 Series)

ITEM	MINIMUM	MAXIMUM
Interphase SMD 4200/ ESDI 4201 controller	1	12
SMD device	1	12
Input/output processor (VIOP)	1	12
Multibus card cage	1	12
Service processor unit (SP2)	1	1
VMEbus control unit (VBCU)	1	12
Memory system (one odd, one even)	1	System Limit
Peripheral interface adapter (PIA)	1	4
CPU utilities (CPX)	1	1

Test Invocation

Test *dev5130* executes under the Diagnostic Shell (Dshell), and supports most of the features of the Dshell. Control of failures is provided by the test since the Dshell does not support multiple drive operations where one drive could fail and yet the subtest should continue on the remaining drives. The Dshell permits the user to initiate subtests in any order. Therefore, each subtest is designed to be independent of all other subtests except in Class 3 which performs system formatting. The default order of subtest execution is from the least complex to the most complex operation.

To invoke the *dev5130* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses in the following figure would appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

CAUTION

Entering only **test dev5130** should never be done on unformatted SMD/ESDI drives since Class 1 and Class 2 tests can overwrite the original Manufacturer's Defect map.

Figure dev5130–1, Test Invocation Sequence

```
(spu)>  cd /mnt/test RETURN
(spu)>  sysreset RETURN
(spu)>  mminit -s RETURN
(spu)>  dshell RETURN

CONVEX DIAGNOSTIC SHELL

: test dev5130 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

NOTE

After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter within this manual.

Entering only **test dev5130** executes all *dev5130* subtests sequentially except Class 4 which must be invoked with the **-c** or **-s** options. The [+> *filename*] option appends all test results to file *filename*.

The following alternate test invocation procedure may be required in some cases.

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev5130–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
: test dev5130 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, the first prompt allows selection of defaults. If the test is run with defaults (by answering **y**, several prompts are skipped and the next prompt displayed is the `Device selection` prompt. If **n** is entered to the first prompt (no defaults are assumed), then a series of prompts are presented. The following figure shows all possible prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. To abort (terminate) the test, enter **^c** (hold down the CTRL key and press **c**) during test execution. All possible prompts and responses are shown in one figure for convenience.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev5130–4, Getting Help During Test Parameter Entry

Character	Description
?	Displays this help menu
d	Displays *DB_diskfmt* file containing the drive parameters
e	Displays entered drive entries
h	Provides help for a specific prompt
i	Displays the */ioconfig* file

After the desired help information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev5130–3, *dev5130* Test Parameter Menu

```
                        ENTER TEST PARAMETERS
          []      Encloses allowed input ranges or values
          ()      Encloses the default value
          ^       Returns to the previous prompt
          :nn     Returns to the prompt # nn
          :       Returns to the first unsatisfied prompt
          :?      Reviews previous entries
 ?          Prints an additional help menu
 1:  Default type (r[read only], w[rite allowed], n[o_defaults])
    [w,r,n]                                              (r) ->
 2:  Are writes to other than the diagnostics cylinder allowed
    [y,n]                                                (n) ->
 3:  Are writes to the diagnostics cylinder allowed
    [y,n]                                                (n) ->
 4:  Number of errors allowed per device each subtest
    [0-65535]                                            (0) ->
 5:  Number of devices failed after which test aborts
    [0-65535]                                           (12) ->
 6:  Threshold for new flaws found during pattern test
    [0-65535]                                            (0) ->
 7:  Verbosity of test [0-31]                            (3) ->
 8:  If pattern testing, start after last completed pattern
    [y,n]                                                (y) ->

            PERIPHERAL CONFIGURATION DATA
      CCU   Chassis  Type     CSR    Int Unit Type
    ------- ------- -------- ------ --- ---- -------
 1) viop 7    0     DKC-204  0x200  2   0   DKD-208
 2) viop 7    0     DKC-204  0xc00  6   0   DKD-214
Enter device 99 to begin user-defined configurations or -1 to end selection
 9:  Device selection [-1,1-2,99]                       (-1) ->
10:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                               (n) ->
11:  Serial number (5 to 31 characters) []
                          (Default: read from drive) ->
12:  Device selection [-1,1-2,99]                       (-1) ->
Enter VIOP -1 to end user-defined configurations
13:  VIOP [-1,3-7]                                      (-1) ->
14:  VMEbus Chassis [0-1]                                (0) ->
15:  Controller Offset in VMEBus [0x0-0xffff]
                                                    (0xe00) ->
16:  Interrupt number [1-7]                              (2) ->
17:  Unit number [0-1]                                   (0) ->
18:  Drive name []                                 (DKD-208) ->
19:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                               (n) ->
20:  Serial number (5 to 31 characters) []
                          (Default: read from drive) ->
Enter VIOP -1 to end user-defined configurations
21:  VIOP [-1,3-7]                                      (-1) ->
22:  Enter OK, or :NN to return to question NN [OK]
                                                        (OK) ->
```

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

A description of the meaning of each prompt follows:

```
Default type (r[read only], w[rite allowed], n[o_defaults])
[w,r,n]                                          (r) ->
```

> **CAUTION**
>
> If **w** is entered to this prompt, then destructive writes are allowed to the entire disk and loss of data and system information is possible.

If **w**, **r**, or RETURN is entered, several test parameter prompts for default selections are skipped and the default values are retained with the exception of the following two prompts:

```
 Are writes to other than the diagnostics cylinder allowed
[y,n]                                            (n) ->
 Are writes to the diagnostics cylinder allowed
[y,n]                                            (n) ->
```

The default values for these prompts are set to **y** if **w** is entered for the **Default type** prompt. They are set to **n** if **r** is entered. The configuration file is then displayed and drive selection begins. Enter **n** to change any of the default parameters.

The following prompts are displayed if the first prompt is answered with **n**:

```
 Are writes to other than the diagnostics cylinder allowed
[y,n]                                            (n) ->
```

If answered with **n** or RETURN, writes are not allowed to cylinders other than the diagnostic cylinder. However, if answered with **y**, writes are allowed to all cylinders with the exception of the diagnostic cylinder which is controlled by the next prompt.

```
 Are writes to the diagnostics cylinder allowed
[y,n]                                            (n) ->
```

If answered with **n** or RETURN, writes are not allowed to the diagnostic cylinder. However, if

answered with **y**, writes are allowed to the diagnostic cylinder.

```
Number of errors allowed per device each subtest
[0-65535]                                    (0) ->
```

If answered with **0** or (RETURN), a device fails if an error occurs during execution of the subtest. However, if answered with a value in the range [**1-65535**], a device fails if the number of errors that occur during the execution of the subtest exceeds this value.

```
Number of devices failed after which test aborts
[0-65535]                                   (12) ->
```

If a value in the range [**12-65535**] or (RETURN) is entered, the test will not terminate unless all devices fail because only 12 devices can be exercised at one time. However, if a value in the range [**0-11**] is entered, the test fails when the number of failed devices exceeds this limit.

```
Threshold for new flaws found during pattern test
[0-65535]                                    (0) ->
```

If **0** or (RETURN) is entered, a device fails if one or more new flaws are detected during pattern test. However, if a value in the range [**1-65535**] is entered, a device fails if the number of new flaws detected during pattern test exceeds this limit.

```
Verbosity of test [0-31]                     (3) ->
```

If **1** or (RETURN) is entered, a summary of all flaws for each drive is printed during Subtest 302, Fix Flaws. In general, verbosity is a sum of values which determines how informative the test is. The values which may be chosen are shown in the following table:

Table dev5130–5, Verbosity Values and Printed Information

VALUE	PRINTED INFORMATION
1	Print summary of bad sectors during Subtest 302, Fix Flaws Subtest
2	Print each grown defect as it is found
4	Print Manufacturer's Defect and Grown Defect list reads
8	Print pattern during the interactive command *pattern_test*
16	Print all errors during the pattern test in Subtest 301, Format and Pattern Subtest

For example, a value of 11 means print the data associated with values of 1, 2, and 8 (1+2+8=11).

```
If pattern testing, start after last completed pattern
[y,n]                                        (y) ->
```

If **y** or (RETURN) is entered, all drives begin pattern test after the last completed pattern. If the drives were previously using different pattern sets or any of the drives had not completed at least pattern 1, then pattern testing is restarted from the beginning on all drives. However, if **n** is entered, then pattern testing is restarted from pattern 1.

The following prompts are displayed if the first prompt is answered with **y**, or after the If

pattern testing, start after last completed pattern prompt is answered:

```
Device selection [-1,1-2,99]                    (-1) ->
```

The range [1-2] in the list of valid inputs corresponds to all the drives listed in the configuration file */ioconfig*. This range varies depending on how many drives are in the */ioconfig* file.

If answered with **-1** or (RETURN), the input is rejected since this is the first request for a device. If answered with one value in the range [**1-2**], then that drive is selected. If at least one drive has already been selected, the value entered must correspond to a different configuration file entry from the entry previously chosen. However, if answered with **99**, all configuration information in subsequent prompts must be manually entered.

The following prompts are displayed if a value in the range [**1-3**] is entered for the `Device Selection` prompt:

```
Previously formatted on CONVEX system with Interphase 4200/4201 controller
[y,n]                                           (n) ->
```

If **n** or (RETURN) is entered, then Class 1 and Class 2 diagnostics format the portions of the disk they need. In Class 3, if the drive has defect lists, then a message is displayed that the disk appears to be previously formatted and a prompt asks whether to continue this drive as a formatted drive. If **n** is entered, the drive is failed. However, if **y** is entered, then Class 1 and 2 diagnostics only perform formatting when the format command is being tested. In Class 3, if the drive does not appear to have defect maps, then a message is displayed that the disk appears to be unformatted and a prompt asks whether to continue this drive as an unformatted drive. If **n** is entered, the drive is failed. The Class 4 subtest ignores the input to this prompt.

```
Serial number (5 to 31 characters) []
                        (Default: read from drive) ->
```

If (RETURN) is entered, then **y** should have been entered to the previous prompt since the serial number must be read from a formatted drive. If **n** was entered to the previous prompt, a serial number is entered at this prompt. If a serial number is entered, it can be from 5 to 31 characters in length and can consist of lower or uppercase characters, numbers, and dashes. Internally, all letters are converted to uppercase so lower and uppercase inputs have the same result.

```
Device selection [-1,1-2,99]                    (-1) ->
```

The range [1-2] in the list of valid inputs corresponds to all the drives listed from the configuration file */ioconfig*. This range varies depending on how many drives are in the */ioconfig* file. If **-1** or (RETURN) is entered, the test exits device selection and asks the user to confirm that all inputs are ok. However, if **99** is entered, then manual inputs of configuration data begins. If one value in the range [**1-2**] is entered, then that drive is selected. If at least one drive has already been selected, the value must correspond to a different configuration file entry from the one previously chosen.

The following prompts are displayed if the `Device Selection` prompt is answered with **99**:

```
VIOP [-1,3-7]                                   (-1) ->
```

If **-1** or RETURN is entered and at least one drive has been chosen, then the user is asked to confirm that all inputs are okay. If no drives have been chosen, then this input (-1) is rejected. If the test is executing on a C1 or C120 machine and one value in the range [**3-7**] is entered, then this value selects the position of the VIOP in the Central Processing Unit (CPU) card cage in the C1 or C120. If the test is executing on a C200 Series machine and one value in the range [**0-3**] is entered, then this value selects the position of the VIOP in the CPU card cage in the C200 Series machine.

```
VMEBus Chassis [0-1]                                    (0) ->
```

If **0** or RETURN is entered, then VMEbus chassis 0 is selected. There are two chassis numbered 0 and 1. If **1** is entered, the second chassis is selected.

```
Controller Offset in VMEbus [0x0-0xffff]
                                                    (0xe00) ->
```

If **0xe00** or RETURN is entered, then the controller which has been set to address 0xe00 is selected. This must be the controller to which the desired drive is attached. Offsets range from 0x0000 to 0xfe00 on 512 byte boundaries (for example, 0x0000, 0x0200, 0x0400, ... etc).

```
Interrupt number [1-7]                                  (2) ->
```

If **2** or RETURN is entered, then interrupt two is used by the controller when an I/O operation completes to interrupt the VIOP. However, if a value in the range [**1, 3-7**] is entered, then this interrupt is used. There is only one requirement when choosing interrupt numbers. Each controller in a VME chassis must have a unique interrupt number. Two controllers in different chassis can use the same interrupt number.

```
Unit number [0-1]                                       (0) ->
```

If **0** or RETURN is entered, then the drive must be set to unit address 0 (usually a switch setting internal to the drive). The cable with the small connector (B cable) from the drive must also be connected to the unit 0 socket on the controller. However, if **1** is entered, then the drive must be set to unit address 1 and the B cable from the drive must be connected to the unit 1 socket on the controller.

```
Drive name []                                       (DKD-208) ->
```

If **DKD-206** or RETURN is entered, then the drive must be an NEC D2352A 520-Mbyte drive. The current alternatives to this drive are the **DKD-208** which is the NEC D2363 1.1-GByte drive and the **DKD-214** which is the Hitachi DK514-38 380-Mbyte Removable Disk Storage (RDS) drive. The RDS drive has an ESDI interface so it must be connected to the Interphase 4201 ESDI controller while the other drives connect to the Interphase 4200 SMD controller.

Any SMD or ESDI drive that works with the Interphase controllers can be used. The drive must be added to the */mnt/bin/lib/DB_diskfmt* file.

```
Previously formatted on CONVEX system with Interphase 4200/4201 controller
[y,n]                                                   (n) ->
```

If the drive is unformatted, has been formatted on any other system than a CONVEX system, or has been formatted with a controller other than an Interphase 4200/4201 controller, then **n** is entered.

> **NOTE**
>
> Previously formatted means that the drive has completed Subtest 300, Format Setup Subtest, not that all of Class 3 subtests have been completed.

If **n** or (RETURN) is entered, then Class 1 and Class 2 diagnostics format the portions of the disk they need. In Class 3, if the drive has defect lists, then a message is displayed that the disk appears to be previously formatted and the user is asked whether to continue this drive as a formatted drive. If **n** is selected, the drive is failed. However, if **y** is entered, then Class 1 and Class 2 diagnostics only do formatting when the format command is being tested. In Class 3, if the drive does not appear to have defect maps, then a message is displayed that the disk appears to be unformatted and the user is asked whether to continue this drive as an unformatted drive. If **n** is entered, the drive is failed. The Class 4 subtest ignores the input to this prompt.

```
Serial number (5 to 31 characters) []
                    (Default: read from drive) ->
```

If (RETURN) is entered, then **y** should have been entered to the last prompt since the serial number must be either provided at this prompt or be read from the drive. If **n** is entered to the previous prompt, the serial number must be entered at this prompt. If a serial number is entered, it can be from 5 to 31 characters in length and can consist of lower or uppercase characters, numbers, and dashes. Internally, all letters are converted to uppercase so lower and uppercase inputs have the same result.

```
VIOP [-1,3-7]                                    (-1) ->
```

If **-1** or (RETURN) is entered and at least one drive has been chosen, then the user is asked to confirm that all inputs are okay. If no drives have been chosen, then this input (-1) is rejected. If the test is executing on a C1 or C120 machine and one value in the range [**3-7**] is entered, then this value selects the position of the VIOP in the Central Processing Unit (CPU) card cage in the C1 or C120. If the test is executing on a C200 Series machine and one value in the range [**0-3**] is entered, then this value selects the position of the VIOP in the CPU card cage in the C200 Series machine.

```
Enter OK, or :NN to return to question NN [OK]
                                                 (OK) ->
```

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

```
**********************************************
* DATA DESTRUCTIVE OPERATION IS ABOUT TO START.*
* VERIFY WRITE-PROTECT IS SET ON ALL DRIVES    *
* EXCEPT THOSE YOU ARE TESTING/FORMATTING.     *
**********************************************
 Then reconfirm that you want to continue [yn] ->
```

If **y** is entered then the actual testing commences with the loading of a driver into the VIOPs and then the execution of subtests begins. However, if **n** is entered, the test terminates and returns to the SPU prompt.

When all prompts have been answered, the screen displays a test parameter summary which echos the prompts that have been answered. The following figure illustrates an example of a "Test Parameter Summary" screen. The actual values and responses vary according to the input.

Figure dev5130–4, Sample Test Parameter Summary

```
              TEST PARAMETER SUMMARY

Default type (r[read only], w[rite allowed], n[o_defaults]) : n
Are writes to other than the diagnostics cylinder allowed
                                                          : n
Are writes to the diagnostics cylinder allowed            : n
Number of errors allowed per device each subtest          : 0
Number of devices failed after which test aborts          : 12
Threshold for new flaws found during pattern test         : 0
Verbosity of test                                         : 3
If pattern testing, start after last completed pattern
                                                          : y
Enter OK, or :NN to return to question NN                 : OK

                        DRIVE CONFIGURATION DATA

       CCU  VME  Cntlr  Int Unit #   # Phys Log Prev
Drive   #    #   CSR  Level #  Cyl Hds Sec Sec Fmtd Name          Serial #
-----  ---  ---  -----  --- --- ---  --- --- --- --- ------- ----------------
   1    7    0   0x200   2   0 1024  27  68  67  no DKD-208 00000
1000    7    0   0xe00   3   0 1024  27  68  67  no DKD-208 99999

Performing sysreset of ccus and memory...
Initializing I/O subsystem and Loading VIOP(s)...
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following message is displayed during hardware initialization:

Figure dev5130–5, Test Initialization Message

```
Performing sysreset...
Initializing I/O subsystem and Loading VIOP(s)...
```

If writes to any of the disks are allowed, the following message is displayed immediately following the summary of inputs:

Figure dev5130–6, Data Destructive Message

```
**********************************************
* DATA DESTRUCTIVE OPERATION IS ABOUT TO START.*
* VERIFY WRITE-PROTECT IS SET ON ALL DRIVES    *
* EXCEPT THOSE YOU ARE TESTING/FORMATTING.     *
**********************************************

Then reconfirm that you want to continue [yn] ->
```

If **y** is entered then the actual testing commences with the loading of a driver into the VIOPs and then the execution of subtests begins. However, if **n** is entered, the test terminates and returns to the SPU prompt.

Figure dev5130–7, Class 3 Test Initialization Message

```
Subtest 300   0:00:00       Prepare for format
```

Before *dev5130* test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The VIOP is booted and loaded
- A driver on the VIOP is started
- VIOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The *dev5130* test contains four classes of subtests as shown in the following table:

Table dev5130–6, *dev5130* Test Classes

CLASS	DESCRIPTION
1	Controller functionality tests
2	Drive functionality tests
3	Drive system format tests
4	Interactive test

The following sections describe the different classes and each of their subtests. Each section contains a table listing each subtest in that class and a description of the subtest. The Class 1 and Class 2 tests verify the controller functionality of the following:

- Reset through VMEbus backplane reset and through Command Status Register
- Used portion of short I/O space
- Invalid command detection and reporting
- Command set coverage includes the following:

Tested commands	Untested commands
Diagnostics	Verify Sectors
Read Long	Reformat*
Write Long	Read Sectors Sequential*
Read Header	Write Sectors Sequential*
Read Raw Data	Verify Sectors Sequential*
Read CDC Flaw Map	Read Sequential, Disable Address Bump*
Report Configuration	Write Sequential, Disable Address Bump*
Write Sector Buffer	Verify Track
Read Sector Buffer	Verify Track Sequentially*
Report Sector ID	Extended Diagnostics*
Format with Sector ID	Dual Port Priority Select*
Initialize Long	Read and Scatter*
Report Configuration Long	Gather and Write*
Read Sectors	Read and Scatter 32*
Write Sectors	Gather and Write 32*
Verify Sectors	Read and Scatter 32 (list 2)*
Format Track	Read and Scatter 32 (list 2)*
Map Track	Buffer Allocation Check*
Handshake	Write After Cache*
Initialize	Clear Drive Fault
Restore	Map Sector
Seek	
Format Track with Data	
Read Noncached	
Track ID	
Fetch and Execute IOPB	

* The commands marked with an asterisk were not available when this diagnostic was designed. They have been recently added. None of these commands are used by the *dev5130* test or by CONVEX UNIX. When a drive faults, the *Restore* command is used to clear the drive fault and rezero the unit instead of using the *Clear Drive Fault* command.

Class 1 Subtests

Class 1 subtests consist of tests which exercise and verify most features of a controller. All of the tests are not data destructive since only the diagnostic cylinder is used for writing. Two options are given at the beginning of the test to specify whether writes to the diagnostic cylinder are allowed and whether writes to cylinders other than the diagnostics cylinder are allowed. These options control which subtests are allowed to run. The following table lists each Class 1 subtest and its description.

Table dev5130–7, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (hr:min:sec)	DATA DESTRUCTIVE
100	Controller Reset	0:00:05	NO
101	Verify Diagnostics Commands	0:00:02	NO
102	Verify Product Identification	0:00:02	NO
103	Verify *Write Sector Buffer* and *Read Sector Buffer* Commands (max throttle)	0:00:02	NO
104	Verify Command Chaining	0:00:03	NO
105	Verify *Initialize* and *Initialize Long* Commands	0:00:03	NO
106	Verify *Format Track* Command and all combinations of interleaves 1 and 2 and skews 0 and 1	0:00:07[1]	YES[2]
107	Verify *Format Sector ID* and *Report Sector ID* Commands	0:00:03[1]	YES[2]
108	Verify *Write Sectors* and *Read Noncached* Commands (all throttle settings)	0:00:15[1]	YES[2]
109	Verify *Format Track with Data* Command	0:00:02[1]	YES[2]
110	Verify *Write Long* and *Read Long* Commands	0:00:04[1]	YES[2]
111	Verify *Read Sectors* Command	0:00:05[1]	YES[2]
112	Verify *Map Track* and *Map Sector* Commands	0:00:03[1]	YES[2]
113	Verify Controller Detects Bad IOPBs	0:00:03	NO

[1] This time will double if two drives are connected to one controller.
[2] Set write protection for drive(s) to prevent loss of data.

Subtest 100, Controller Reset

Subtest 100 performs a VMEbus chassis reset and verifies that the controller's Command Status Register (CSR) contains a 0x4000 pattern. Then the LED bit (0x8000) is set and read back to ensure it was set. The BDCLR bit in the CSR (0x2000) is set which resets the controller. Then the CSR is verified to indicate that it contains a 0x4000 pattern. The one bit that is on in this pattern is the board OK bit which is the controller's way of indicating it has passed its internal diagnostics.

Subtest 101, Verify Diagnostics Commands

Subtest 101 performs each controller's diagnostics test using interrupts to respond to each controller's completion of a diagnostics command. The command's completion is verified by receiving an interrupt and checking that the board OK bit in the controller's CSR is set.

> **NOTE**
>
> The returned status and error codes for the remaining commands are checked in the Input/Output Parameter Block (IOPB) for correctness.

Subtest 102, Verify Product Identification

Subtest 102 executes a controller *Handshake* command which returns the controller's product code, product variation, revision level, month, day, and year. This information is printed each time the subtest is run. If the information fails gross range-checking, the Input/Output Parameter Block (IOPB) indicates that an error has occurred, or if the release date of the firmware is older than the oldest acceptable firmware date, then the controller and all attached drives fail.

Subtest 103, Verify *Write Sector Buffer* and *Read Sector Buffer*

Subtest 103 performs writes to and reads from one sector buffer in the controller's memory with an all '1's pattern and then an all '0's pattern. After the buffer is read, the data is compared. The throttle setting is set to 512 bytes per DMA burst which is the maximum amount of data that can be transferred in one controller *Write Sector Buffer* or controller *Read Sector Buffer* operation.

Subtest 104, Verify Command Chaining

Subtest 104 verifies command chaining by performing chained controller *Write Buffer* and controller *Read Buffer* commands.

> **NOTE**
>
> The throttle setting is 64 bytes per DMA burst which is the size of the cache on the VIOP. This is the size of all DMA bursts in Subtests 104 though Subtest 400 except Subtest 108.

Subtest 105, Verify *Initialize* and *Initialize Long*

Subtest 105 sets up a unit initialization block in VIOP memory and performs a controller *Initialize* command to load various device parameters into the controller. The subtest then uses the

controller *Report Configuration* command to verify the initialization. It then performs a controller *Initialize Long* command and verifies it using the controller *Report Configuration Long* command. All subsequent subtests use the *Initialize Long* command to initialize the controller. CONVEX UNIX also uses the *Initialize Long* command to perform controller initialization.

Subtest 106, Verify *Format Track* and all Combinations of Interleaves

Subtest 106 executes the controller *Format Track* command to format all tracks on the diagnostic cylinder. The tracks are formatted with interleaves of 1 through 16 while using a skew of 0. Then skews of 0-15 are performed with interleave first set to 1 and then set to 2. Each of these 48 tests is verified by reading the track headers with the controller *Track ID Read* command and comparing the track headers to the expected headers.

Subtest 107, Verify *Format Sector ID* and *Report Sector ID*

Subtest 107 verifies the controller *Format Sector Id* and controller *Report Sector Id* commands. First, track 0 of the diagnostic cylinder is formatted. Then a controller *Report Sector Id* command is performed on one track of the diagnostic cylinder and the headers are written out in reverse order using the controller *Format Sector Id* command. Then the format of the headers is verified by performing another controller *Report Sector Id* command and verifying the headers are reversed. Finally, the track is restored by another *Format Track* command.

Subtest 108, Verify *Write Sectors* and *Read Noncached*

Subtest 108 verifies the controller *Write Sectors* and *Read Noncached* commands. First, a *Format Track* command is performed on one track on the diagnostic cylinder. Then the *Write Sectors* and *Read Noncached* commands are verified by performing writes to the minimum sector on the track. Then using the multiple sector technique, writes are performed to the minimum + 1 sector and minimum + 2 sector. Then reads are performed on the minimum sector using single sector I/O and then reads are performed on the next two sectors using multiple sector I/O. Next, a verify is performed to ensure that the data written was read back successfully. These operations (except for the format track) are repeated for each throttle setting (4, 8, 16, 32, 64, ... 512 bytes per transfer to and from main memory). If other controllers are available, the above steps are repeated on the other controllers.

Subtest 109, Verify *Format Track with Data*

Subtest 109 verifies the *Format Track with Data* command. The *Format Track* command is used to format track 0 of the diagnostics cylinder by writing '0's to sector 0. Then the *Format Track with Data* command reformats the track with a `0x9abcdef0` repeating pattern. Then sector 0 is read and compared. The first four bytes of the sector are altered when formatted to reflect the cylinder, head and sector address of the sector. Then the first four bytes are verified.

Subtest 110, Verify *Write Long* and *Read Long*

Subtest 110 verifies *Write Long* and *Read Long* commands by reading data and Error Correction Code (ECC) information from each drive and then writing the data and information back to the drive. Before beginning, the subtest performs a *Format Track* command if needed on track 0 of

the diagnostic cylinder. The minimum sector and the next sector are written to with test patterns `0x00000000` and `0xffffffff` respectively and then the sectors are read using two *Read Long* commands. The headers and data fields are verified and the data and ECC information are swapped between the two sectors. The *Write Long* command is used to write the sectors back out and then the *Read Sectors* command is used to read the data back from the two sectors. The data should be in the opposite sectors corresponding to the sectors where the data was originally written.

Subtest 111, Verify *Read Sectors*

Subtest 111 verifies the *Read Sectors* command. The *Write Sectors* command is used to write to the first two cylinders. Then the *Read Sectors* command is used to read the two cylinders. The subtest is repeated for all default patterns (refer to Subtest 301, Format and Pattern Test for patterns).

Subtest 112, Verify *Map Track* and *Map Sector*

Subtest 112 verifies the *Map Track* and *Map Sector* commands. Two tracks on the diagnostic cylinder are formatted using the *Format Track* command and then sector 0 of the first track is mapped to sector 0 of the second track with the *Map Sector* command. Then the first sector is read and verified that the first word contains the address of the second sector in the first word (written by the *Format Track* command).

Then the two tracks are reformatted using the *Format Track with Data* command and the first track is mapped to the second track using the *Map Track* command. Then the sectors on the first track are read. The first word of each sector should contain the address from the second track (written by the *Format Track with Data* command).

Next, the first track is reformatted.

Subtest 113, Verify Controller Detects Bad IOPBs

Subtest 113 verifies the controller is capable of detecting bad Input/Output Parameter Blocks (IOPBs). A head address outside the controller's limit is sent to the controller for checking. The controller should reject the address. Then a cylinder address outside the drive's range is sent to the controller. The controller should also reject the cylinder address

Class 2 Subtests

Class 2 subtests consist of tests which exercise drives to verify that they are mechanically and electrically functional.

The Class 2 subtests verify the drive functionality of the following:

- Write and read every head
- Single and multi-track seeks

- Fault condition detection

The following table lists each Class 2 subtest and its description.

Table dev5130–8, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME[3] (hr:min:sec)	DATA DESTRUCTIVE
200	Verify Head Switching	0:00:42[1]	YES[2]
201	Verify Sequential-Track Seeks	0:00:30[1]	YES[2]
202	Perform Min-to-Max Track Seeks	0:00:20[1]	NO
203	Perform Accordion Seeks	0:01:00[1]	NO
204	Perform Random Seeks	0:01:00[1]	NO
205	Verify Detect of Forced Faults (cylinder and head)	0:00:30[1]	NO

[1] This time will double if two drives are connected to one controller.
[2] Set write protection for drive(s) to prevent loss of data.
[3] Times shown are for one Hitachi DK514-38 drive.

Subtest 200, Verify Head Switching

Subtest 200 verifies head switching and also verifies that each head can write and read. Special formatting takes place for Class 2 subtests, if necessary, before the main portion of this subtest executes. The controller *Write Sectors* command is used to write to each sector of each track on the diagnostic cylinder. A controller *Read Noncached* command is used to read the data and then the write and read buffers for each sector are compared. First a `0x0000` pattern is used and followed by a `0xffff` pattern. The *Write Sectors* command and the *Read Noncached* command, and the compare are repeated ten times.

Subtest 201, Verify Sequential-Track Seeks

Subtest 201 verifies sequential-track seeking by first formatting head 0 on all cylinders (if writing is allowed). Then a controller *Report Sector ID* command is performed on head 0 of each cylinder starting with cylinder 0 to verify positioning.

Subtest 202, Perform Min-to-Max Track Seeks

Subtest 202 performs min-to-max track alternate seek. Special formatting takes place for Class 2 subtests, if necessary, before the main portion of this subtest executes. A controller *Track ID Read* command performs an implied seek to the minimum track. After the test verifies the cylinder number, a controller *Track ID Read* command performs an implied seek to the maximum track. When this cylinder is verified, the seek repeats to the minimum and maximum track 100 more times with verification at each track. Then the seek repeats, using the controller *Seek* command with no verification until the seek is complete. To complete the test, a controller *Track ID Read* command is used to read the last track and positioning is verified.

Subtest 203, Perform Accordion Seeks

Subtest 203 performs an accordion seek on a drive. Special formatting takes places for Class 2 subtests, if necessary, before the main portion of this subtest executes. A controller *Track ID Read* command performs an implied seek to the minimum track, maximum system track, min+1, max-1, min+2, max-2, etc., until a one-track seek is performed. The test verifies the seek by checking each of the headers just read. The accordion seek then repeats using the controller *Seek* command with no verification. After the last seek is performed, a controller *Read Header* command is performed to verify the final positioning. The test chains commands to two drives on a controller if both drives are connected to one controller.

Subtest 204, Perform Random Seeks

Subtest 204 performs 1000 random seeks within the specified minimum and maximum cylinders on a drive. Special formatting takes places for Class 2 subtests, if necessary, before the main portion of this subtest executes. Random numbers are created by initializing C's random number generator (*rand*) with a seed value of 113 and then calling *rand* for successive numbers. The controller *Track ID Read* command is used for implied seeks which verify positioning. The test then performs the random seek using the controller *Seek* command with no verification until the seeks are complete. Then a controller *Read Header* command is used to verify the last cylinder. The test chains commands to two drives on a controller if both drives are connected to one controller.

Subtest 205, Verify Detect of Forced Faults

Subtest 205 verifies the ability of the SMD drives to detect fault conditions. A controller *Initialize* command is used to set the head and cylinder limits to two greater than the maximum values specified in the file */mnt/bin/lib/DB_diskfmt*. Then a controller *Read Sectors* command is used to read a track from a cylinder that is two greater than the maximum. This generates a seek error. An error may not occur if the number of cylinders specified in */mnt/bin/lib/DB_diskfmt* is incorrect or if the drive has exactly 1023 or 1024 cylinders. The subtest expects certain errors or no errors since all known drives are characterized. For future drives, an `Expected error did not occur` error should be displayed if a drive fault or seek error does not occur.

Next, the test sets the head to two greater than the maximum value and then a controller *Write Sectors* command is used to write to this head on the diagnostic cylinder. This generates a write fault. After the write fault, the error does not clear until a drive reset is performed. The test performs a read of head 0 of the diagnostic cylinder and verifies that the write fault still exists. Then the test resets the drive and reads head 0 again; the write fault should no longer exist.

Class 3 Subtests

Class 3 subtests consist of tests which format new drives or reformat previously formatted drives for system use. The following table lists each Class 3 subtest and its description.

Table dev5130–9, Class 3 Subtests

SUBTEST	DESCRIPTION	TIME (hr:min:sec)	DATA DESTRUCTIVE
300	Format Setup	N/A	YES[3]
301	Format and Pattern Test	2:30:00[1]	YES[3]
302	Fix Flaws	0:01:00	YES[3]
303	Initialize Diagnostic Cylinder	0:04:00[2]	YES[3]
304	Verify System Format	0:08:00	NO
305	Verify Diagnostic Cylinder	0:00:30[2]	NO
306	Verify Pattern Test Error Threshold	0:00:02	NO

[1] Time varies depending on the types of drives and number of drives per controller. For one drive, the times are the following:

NEC 2352 (1/2 GByte) -> 1.25 hours
NEC 2363 (1 GByte) -> 2.30 hours
Hitachi 514-38 (RDS drive) -> 1.00 hours

Two drives on one controller will double these times.
If drive types are mixed, use the longer time.

[2] Multiply this time by the number of drives being formatted.

[3] Set write protection for drive(s) to prevent loss of data.

Subtest 300, Format Setup

Subtest 300 provides an interactive means of changing the way disks are formatted and also allows the user to input/edit flaw location information.

First, the subtest attempts to read the Manufacturer's Defect (MD) list and Grown Defect (GD) list on the innermost cylinder. If a MD list is not available, then the subtest sees if the file */mnt/usr/backup_maps/bkup.s* exists where *s* is the last five characters of the drive's serial number. If so, this copy is used.

First, the following initialization message for Subtest 300 is displayed:

Figure dev5130–8, Subtest 300 Initialization Message

```
Subtest 300   0:00:00       Prepare for format
```

Next, the following interactive prompt is displayed:

Figure dev5130–9, Subtest 300 Interactive Prompt

```
Type 'h' for help with commands
format setup (D1;Defect)->
```

If **h** is entered, a help facility is displayed which lists the available commands. The help display is shown in the following figure:

Figure dev5130–10, Subtest 300 Help Screen

```
Commands:
q[uit]                      - terminate the test and return to UNIX prompt
c[hange_mode]               - toggles logical sector/defect map entry mode
co[ntinue]                  - exit setup and continue with format
cyl hd sec                  - logical sector to be slipped
cyl hd bcai len             - defect map entry to be slipped
de[lete] cyl hd sec         - delete logical sector entry
de[lete] cyl hd bcai len    - delete defect map entry
d[rive] [n]                 - change/display current drive
f[ile] filename             - get inputs from specified file
fo[rmat_options]            - allows you to modify the format
h[elp]                      - display this information
l[ist] [{m,g,n,needs}]      - list all, manu[m], grown[g], new[n], needs
m[ap_track] cyl hd          - maps a track to an alternate
no_f[law_map]               - to inform formatter that no flaw map exists
no_t[rack_flaw] cyl hd      - used when no flaw data exists for a track
!unix-command               - execute unix command
'comment                    - comment; echoed to screen
```

Subtest 300, *change_mode* Command

c[hange_mode]

When manually entering defects, first select the entry mode. The default mode is Byte-Count-After-Index (BCAI) mode. To enter defects as logical sectors, modes must be switched with the *change_mode* command. Then enter the position of each flaw. In sector mode, this means typing the cylinder, head, and sector where the flaw exists. In BCAI mode, enter the cylinder, head, byte-count-after-index, and bit-length.

The input mode (logical sector or defect map mode) is revealed in the slip prompt as shown in the following figure:

Figure dev5130–11, Changing Input Modes

```
format setup (D1;Sector)->c
format setup (D1;Defect)->
```

Subtest 300, *continue* Command

co[ntinue]

The *continue* command is used to exit setup and continue with the format. When all inputs have been entered, type **continue**. Before Subtest 300, Format Setup exits, it will read the original Manufacturer's Defect (MD) maps from all drives for which no MD lists already existed and for which no backups existed.

Any drives which had no MD list on the innermost cylinder or backup file but did have original MD maps now have backup files containing the data from the original MD maps. The name of the files are */mnt/usr/backup_maps/bkup.s* where *s* is the last 6 digits of each drive's serial numbers.

For those drives that did not have a valid MD list or GD list, the defect cylinder (the cylinder where MD and GD lists are recorded) is formatted, pattern-tested and flaws remapped. Then the MD and GD lists for these drives are written to the drives. Subtest 300 then exits.

Refer to the *list*, *no_flaw_map*, and *no_track_flaw* commands for more information.

Subtest 300, *cyl hd bcai len* and *cyl hd sec* Commands

cyl hd bcai len

or:

cyl hd sec

The *cyl hd bcai len* command allows a defect map entry to be slipped. The *cyl hd sec* command allows a logical sector to be slipped. When a defect is entered, a list of logical sectors that correspond to the defect is generated as follows:

Figure dev5130–12, List of Logical Sectors For a Defect

```
format setup (D1;Defect)-> 293 1 572 9510
        Associated logical sectors: 59 0 1
```

The figure illustrates that three sectors are affected by the media flaw which starts at byte 572 from index and is 9510 bits long.

If two defects exist that affect the same sector, the logical sector will only be entered once. Subsequent entries of the same sector will result in the message:

```
This entry already exists (ignored)
```

For instance, given the following two defects:

cylinder	head	bcai	bit-length
10	0	70	1
10	0	80	1

Both defects fall in sector 0 so when the second defect is entered, it will not create a new entry in the input list.

Subtest 300, *delete* Commands

de[lete] *cyl hd sec*

or:

de[lete] *cyl hd bcai len*

The *delete* command is used to delete a logical sector entry or a defect map entry. An example of entering a bad location and deleting it is shown along with the *list* command in the following figure:

Figure dev5130–13, Entering and Deleting an Incorrect Location

```
format setup (D1;Sector)-> 17 7 23
format setup (D1;Sector)-> 17 7 46
format setup (D1;Sector)-> del 17 7 46
        Input 17 7 46 has been removed
format setup (D1;Sector)-> list

Summary of flaws on drive 1 serial number 003013
 CYL HD SEC   BCAI   LEN TYPE  ERR SRC | CYL HD SEC   BCAI   LEN TYPE  ERR  SRC
  17  7  23  35032  4825      NONE USR |
```

As shown in the previous figure, use the *list* command to display inputs and defect list entries and with the *delete* command delete any incorrect entries except MD list entries (refer to the *list* command in Subtest 400, Interactive Test for more information about listing flaws). MD list entries are marked with MAP in the SRC column of a list.

Subtest 300, *drive* Command

d[rive] [*n*]

The *drive* command is used to change or display the current drive. If a drive is not specified, a list of all selected drives is displayed and a prompt is displayed to enter a drive number. An example of switching drives follows:

Figure dev5130–14, Switching Drives Using the *drive* Command

```
format setup (D1;Sector)-> d 2
        Drive 2 is now selected
```

Subtest 300, *file* Command

f[ile] *filename*

To enter the defect data from one or more files, select each file by typing:

file *filename*

where *filename* is the actual name of the file. The first line of the file defines the drive type and looks like this:

n *drivename*

where *drivename* is the drivename which can be found in */mnt/bin/lib/DB_diskfmt* on the Service Processor (for example, DKD-208 for the 1 GByte NEC 2363 drive). Following the drive name line, a file has remaining lines contain either BCAI inputs or logical sector inputs. A BCAI input is preceded with the letter **d** while a logical sector input is preceded with the letter **s**. The spare sector can be specified by using a logical sector number one greater than the last used sector number.

To specify a track that is to be mapped to an alternate track, use the letter **m** followed by the cylinder and head of the bad track. One or more spaces separate each item in the file and a new line can be started between any two items. To include comments in the file type a # at any place on a line. Everything from the # to the end of the line is ignored. Blank lines are also allowed. A file containing defect data is shown in the following figure:

Figure dev5130–15, Creating a Defect Data File

```
#------------------------------ start of file ----------------------------
# serial number: 003013
n  DKD-206
#   cyl  hd   bcai  len       cyl  hd   bcai  len  # NEC 2352 drive
d   157  15  24395   34    d  297  14  14102    4  # BCAI Inputs
d   466   0    206    1

#   cyl  hd  sec             cyl  hd  sec
s   457  12   42          s  821   5   11         # Logical sector inputs

#   cyl  hd
m   622  14                                      # map track input
#------------------------------ end of file ------------------------------
```

Defect input mode only applies to manual inputs. File inputs are controlled by the character that precedes the defect location.

Subtest 300, *format_options* Command

fo[rmat_options]

The *format_options* command is used to modify the format of the drive. To manipulate usage of the MD list or GD list, type **format_options**. Several prompts must be answered in response to this command. The prompts are displayed in the following figure:

Figure dev5130–16, Prompt Display for the *format_options* Command

```
For Drive 1 on controller (viop/vb/csr) 7/0/e00:
     Wipe out defect lists if they exist [yn] (n) -> RETURN
     Use manufacturer's defects during slip of sectors [yn] (y) -> RETURN
     Keep old grown defects  [yn] (y) -> RETURN
               - if 'n', next question will be asked
     About to delete grown defects. Continue  [yn] (y) -> RETURN
```

The defaults are in effect unless changed.

> **NOTE**
>
> If a drive is being reformatted, the use of the Manufacturer's Defects will be the same as the last time it was formatted unless this command is used to change them.

Subtest 300, *help* Command

h[elp]

This command lists the commands and their arguments.

Subtest 300, *list* Command

l[ist] [{**m,g,n,needs**}]

The *list* command is used to list all manufacturer defects, grown defects, new defects, or defect needs. If the currently-selected disk has been previously formatted, then the MD list and GD list will already be read when the first prompt appears. This data can be listed using the *list* command. If the drive is unformatted, the original manufacturer's defect map is read when exiting setup. If defect needs were listed after the *continue* command, type **list needs** to redisplay the current needs.

Figure dev5130–17, Using the *list* Command

```
format setup (D2;Sector)-> list

Summary of all flaws on drive 2 serial number 003418
 CYL HD SEC   BCAI   LEN TYPE  ERR SRC | CYL HD SEC   BCAI   LEN TYPE  ERR SRC
 100  5  52  10536     1       NONE USR | 257  9  35  26401  1392       NONE USR
 257  9  58  26576   600       NONE USR |

format setup (D2;Sector)->
```

Subtest 300, *map_track* Command

m[ap_track] *cyl hd*

To map an entire bad track, use the *map_track* command. The test selects one of the alternate tracks for use.

Subtest 300, *no_flaw_map* and *no_track_flaw* Commands

no_f[law_map]

or:

no_t[rack_flaw] *cyl hd*

The *no_flaw_map* command is used to inform the formatter that no flaw map exists. The *no_track_flaw* command is used when no flaw data exists for a track. After using the *continue* command, if no defects were readable from anywhere or some of the original MD map was unreadable, then the user is prompted to enter the needed defect data. These inputs can come from a file of defects or from manual inputs. If inputs do not exist to satisfy the listed needs, then use one of the two commands to satisfy the test. To cancel a need for inputs due to an

unreadable map type **no_flaw_map**. To cancel a need for a specific track type **no_track_flaw** *cyl hd* where *cyl hd* is the track for which a need was listed.

Subtest 300, *quit* Command

q[uit]

The *quit* command is used to terminate the test and return to the UNIX prompt. The prompt in the following figure is displayed when the **quit** command is issued:

Figure dev5130–18, Executing the *quit* Command Within Subtest 300

```
format setup (D2;Sector)->quit
        Are you sure you want to terminate the test [yn] (y) ->
```

Subtest 300, Execute UNIX Command

! *UNIX Command*

The *!* (UNIX command) is used to execute a UNIX command while within Subtest 300. An example of its use is displayed in the following figure:

Figure dev5130–19, Executing a UNIX Command Within Subtest 300

```
format setup (D2;Sector)-> !cat def_003418     <-to illustrate unix cmd
# Serial Number: 003418
n DKD-206
d  100  5 10536     1
d  257  9 26401  2000
```

Subtest 300, Enter Comments

'comment

This command is used to enter a comment. To enter a comment, type the ' command and a comment. The comment is echoed so it is redirected output. This is useful to document redirected output.

Subtest 301, Format and Pattern Test

Subtest 301 formats a drive and pattern tests all sectors except the ones in the defect list cylinder. This includes sectors that will later be used as spares. The patterns used for pattern testing are listed in the following table:

Table dev5130–10, Patterns for Pattern Testing

SET	PATTERN	
1	MFM Data Encoding	
	0x00000000	0x6DB66DB6
	0xFFFFFFFF	
	0x55555555	
	0xAAAAAAAA	
2	2-7 RLL Data Encoding	
	0x00000000	0x9ABCDEF0
	0xCCCCCCCC	0xAF5BAF5B
	0x88888888	0x22222222
	0xBCDEF09A	
3	1-7 RLL Data Encoding	
	0x00000000	0x9ABCDEF0
	0xCCCCCCCC	0xAF5BAF5B
	0x88888888	0x22222222
	0xBCDEF09A	
4	Combination of Unlike Drives	
	0x6db66db6	0xffffffff
	0x9abcdef0	0xcccccccc
	0x00000000	0x33333333
5	User Specified Patterns	
	Patterns in *dev5130.patt* file	

If all drives that are to be formatted use the same encoding scheme, then the corresponding set of patterns will be used. However, if drives with different encoding schemes are formatted together, then pattern set 4 is used.

These default patterns can be replaced by up to 15 other patterns if the file *dev5130.patt* is created in the current directory or if it is created in */mnt/bin/lib*. The current directory is searched first. Each pattern is preceded with a 'p' and at least one space, tab or newline character. The pattern can be from 1 to 1024 hex characters per pattern (upper or lowercase letters are allowed). More than one line can be used to define the patterns. Blank lines are also allowed.

The following is an example of two patterns in a *dev5130.patt* file:

```
p A    p 23456789a
```

The first pattern is expanded so that every byte written contains a 0xAA pattern. The second

pattern has 9 hex digits which are repeated when written. The following is the resulting data:

23456789 a2345678 9a234567 89a23456 789a2345 6789a234 56789a23 456789a2
---------- etc ----------

Any sector-related errors (header errors; hard Error Correction Code (ECC) error; or correctable ECC error) are retried immediately and, if an error occurs again in ten retries (does not have to be the same error), the sector location is saved for later slipping. Errors that do not repeat are discarded. A maximum of 2048 errors can be saved per drive. This includes the flaws from Subtest 300, Format Setup and any found during pattern test. If a verbose value of 16 is selected during test parameter inputs, each error is printed at the time it is detected. A verbose value of 2 results in only grown defects being printed. The last operation in Subtest 301, Format and Pattern Test writes the MD and GD lists.

Subtest 302, Fix Flaws

If the innermost cylinder does not yet contain the new Manufacturer's Defect (MD) list, then the drive fails.

If Subtest 301 Format and Pattern Test was not run, then the drive is formatted with one spare sector per track. Then all sectors which have been marked bad will be slipped. If more than one sector is bad on a track or a header-related error occurred on the track, the entire track is remapped to an alternate track. The number of cylinders worth of spare tracks for a particular drive is defined in the *DB_diskfmt* file.

If verbose value 1 is selected during the test parameter menu (this is the default along with printing each grown defect as it is found), a summary of bad sectors and tracks for each drive will be printed before slipping occurs.

The last operation writes the MD and GD lists.

Subtest 303, Initialize Diagnostic Cylinder

Subtest 303 writes special patterns to the diagnostic cylinder which is the cylinder just before the defect list cylinder. Sector zero of each track contains a table of contents describing what is written to each of the remaining sectors. If no sectors have been relocated on a track, sector 1 is marked bad. The next twelve sectors contain Error Correction Code (ECC) errors of length 1 to 12 respectively. The remaining sectors have the patterns listed in Subtest 301, Format and Pattern Test written to them. Sector 13 (or 14 if sector 1 is marked bad) will contain the first pattern, sector 14 (or 15) will contain the second pattern, and so on with the patterns repeating throughout the remaining sectors of each track.

Subtest 304, Verify System Format

Subtest 304 reads all five copies of the original Manufacturer's Defect (MD) list, Grown Defect (GD) list, and track map log and verifies that at least three of each are good. If not, the test fails.

Then the subtest reads every logical sector in the usable portion of the disk. Any errors are reported since all bad sectors should be relocated and be handled by the controller.

Any errors are reported and do count against the device errors per subtest limit. If the number of errors exceeds the limit, the drive is failed. The usable portion of each drive is all cylinders preceding the alternate track area and any used alternate tracks.

Subtest 305, Verify Diagnostic Cylinder

Subtest 305 reads each sector on the diagnostic cylinder and expects soft or hard Error Correction Code (ECC) errors on sectors 1 through 12 of each track (or sectors 2 through 13 if sector 1 was marked bad). The remaining sectors are read with data compare and must be error-free.

Subtest 306, Verify Pattern Test Error Threshold

A threshold can be set during user prompts which will determine how many new errors can be detected during Subtest 301, Format and Pattern Test pattern testing before this subtest fails. The intention is that all errors detected by pattern test should already be in the MD map. If the errors are actually new, this may indicate an unacceptable degradation of the disk since it was tested at the manufacturer or inaccuracy in manufacturer's media tester.

Class 4 Subtest

The Class 4 subtest consists of one test, the interactive test, which allows the user to read and display sectors, verify parts of disks, format single tracks, slip sectors, etc.

Table dev5130–11, Class 4 Subtest

SUBTEST	DESCRIPTION	TIME (hr:min:sec)	DATA DESTRUCTIVE
400	Interactive Test	N/A[1]	YES[2]

[1] The time for the interactive test depends on the operations performed.
[2] Set write protection for drive(s) to prevent loss of data.

Subtest 400, Interactive Test

Subtest 400 provides a special interactive test interface to allow the user to perform a variety of disk maintenance tasks such as pattern-testing portions of the disk, slipping bad sectors, formatting single tracks, and several other useful operations. Help information is available when needed.

> **CAUTION**
>
> Five of the commands are potentially data destructive: *pattern_test*, *slip_sectors*, *format*, *data_verify*, and *copy_from_spu*.

The first four commands do an automatic save of the data the command is going to overwrite before the operation begins with the following exceptions:

- An attempt to pattern test more than one track is performed and **y** is entered when asked to confirm multiple track pattern test (because only one track can be saved).
- An attempt to preserve a track's data before a destructive operation fails and a response is entered to force the operation anyway.
- The pattern test, slip sectors, or format operation has completed and then data errors occur during the restore of the track's data.
- The keys CTRL and **c** or CTRL and **b** are pressed in the middle of the operation.
- Automatic saving is disabled by using the command *toggle_save*.
- A power outage or some other unforeseen event causes the test to abort in the middle of the operation.

The fifth command, *copy_from_spu* restores data to the drive which has been saved using *copy_to_spu*. Since it writes to the disk, it can be destructive. However, the usual way this could corrupt data is if the temporary file created by *copy_to_spu* is edited before using *copy_from_spu* to restore the data.

Subtest 400, Interactive Test Invocation

To invoke the *dev5130* interactive test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The [+> *filename*] option appends all test results to file *filename*. The prompts and responses in the following figure would appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

To invoke the test, use the procedure shown in the following figure:

Figure dev5130–20, Subtest 400 Interactive Test Invocation Sequence

```
(spu)>sysreset; mminit -s; dshell RETURN
CONVEX DIAGNOSTIC SHELL
: test dev5130 -s 400 [+> filename] RETURN
```

Subtest 400, Interactive Test Menu

Once the test is invoked, prompts are displayed to specify various options. The following figure shows typical prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All the prompts and responses are shown in one figure for convenience.

Figure dev5130–21, Subtest 400 Interactive Test Parameter Menu

```
                ENTER TEST PARAMETERS
       []     Encloses allowed input ranges or values
       ()     Encloses the default value
       ^      Returns to the previous prompt
       :nn    Returns to the prompt # nn
       :      Returns to the first unsatisfied prompt
       :?     Reviews previous entries
Default type (r[read only], w[rite allowed], n[o_defaults])
[w,r,n]                                        (r) ->

              PERIPHERAL CONFIGURATION DATA
     CCU     Chassis   Type      CSR    Int  Unit  Type
    -------  -------  --------  -----  ---  ----  -------
 1)  viop 3     0     DKC-204   0xc00   1     0   DKD-206
 2)  viop 3     0     DKC-204   0xa00   4     0   DKD-208
 3)  viop 6     1     DKC-203   0xc00   3     0   DKD-214

Enter device 99 to begin user-defined configurations or -1 to end selection
 2:  Device selection [-1,1-3,99]                    (-1) ->1
 3:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                          (n) ->y
 4:  Serial number (5 to 31 characters) []
                          (Default: read from drive) ->RETURN
 5:  Device selection [-1,1-3,99]                    (-1) ->2
 6:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                          (n) ->y
 7:  Serial number (5 to 31 characters) []
                          (Default: read from drive) ->RETURN
 8:  Device selection [-1,1-3,99]                    (-1) ->3
 9:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                          (n) ->y
10:  Serial number (5 to 31 characters) []
                          (Default: read from drive) ->RETURN
11:  Device selection [-1,1-3,99]                    (-1) ->RETURN
12:  Enter OK, or :NN to return to question NN [OK]
                                                   (OK) ->RETURN

***********************************************
* DATA DESTRUCTIVE OPERATION IS ABOUT TO START.*
* VERIFY WRITE-PROTECT IS SET ON ALL DRIVES    *
* EXCEPT THOSE YOU ARE TESTING/FORMATTING.     *
***********************************************

Then reconfirm that you want to continue [yn] ->y
```

As shown in the previous figure, enter **y** to the first prompt. Then select a drive to test at the `Device selection` prompt and always enter **y** to the `Previously formatted` prompt and always enter RETURN to the `Serial number` prompt. This drive selection process may be repeated for additional drives.

When all drives to be tested have been selected, press RETURN twice to select the defaults to the `Device selection` and `Enter OK` prompts. Then enter **y** to the `Then confirm` prompt to allow the test to continue. After a minute, the interactive test will start up.

Subtest 400, Interactive Test Mode

Once test initialization is complete (typically takes less than one minute), the following is displayed:

Figure dev5130–22, Subtest 400 Interactive Test Mode

```
                    INTERACTIVE TEST MODE
                    FOR SMD AND ESDI DRIVES

Type 'h' for help
(D1;Save)->
```

NOTE

D1 means drive 1 is selected and Save means that save of track data is automatic during the destructive commands *format, pattern_test, data_verify* and *slip_sectors.*

Type **h** at any time to display the list of available commands.

To exit the interactive test, type **q** and press RETURN. If a track is saved, a prompt asks if it is okay to lose this data. If **y** is entered or if a track is not saved, *dev5130* ends normally and exits back to the *dshell* prompt. If **n** is entered, test execution returns to the interactive prompt with nothing changed.

NOTE

When the interactive test is exited, the drives under test will ALWAYS show PASSED in the summary. This is because all failures are ignored during the interactive test.

Subtest 400, Interactive Test Commands

The following table lists all the available interactive test commands. Also a brief description of each command's purpose is listed. For the exact syntax of each command, refer to the command's description in the following section.

Table dev5130–12, Subtest 400 Interactive Test Commands

COMMAND	DESCRIPTION
a[lternate_seek]	Seek between two selected cylinders
copy_f[rom_spu]	Restore sectors from service processor disk to SMD
copy_t[o_spu]	Write sectors from SMD to service processor disk
da[ta_verify]	Write once, repetitively read and compare
dr[ive_select]	Select drive
du[mp_lists]	Dump defect lists to service processor disk
fo[rmat]	Reformat one track
hd[e_display]	Display header, data, and ECC
h[elp]	Display list of commands and arguments
l[ist]	Display list of flaws
pa[ttern_test]	Pattern test range of sectors
pr[otection]	Enable or disable write protection
q[uit]	Exit Interactive Test
res[tore_track_data]	Restore previously saved track data
sa[ve_track_data]	Save one track of data
sec[tor_display]	Display data from range of sectors
ser[ial_number]	Display or change disk serial number
sl[ip_sectors]	Slip one or more sectors
st[atus]	Display information about device
to[ggle_save]	Enable and disable automatic save
tr[ack_headers_display]	Display track headers
v[erify_format]	Verify a range of sectors
!*UNIX-command*	Execute UNIX command
'*comment*	Comment; ignored

Each command can be executed by entering the portion of the command that precedes the brackets or by entering all of the command. For example, the *quit* command can be executed by entering **q** or **quit**. The following sections describe the different interactive test commands.

Subtest 400, Seek Between Two Selected Cylinders

a[lternate_seek] [*nnn* **times**] *min-cyl* **to** *max-cyl*

This command provides the capability of performing alternate seeks between two cylinders so adjustments can be made to drives. Seeks are between the two specified cylinders to head. Data is not transferred during the seeks.

Arguments:

- [*nnn* **times**] — Repetition count. Possible values include:
  - **1** — Lower bound value, default value
  - **2,147,483,647** — Upper bound value
- *min-cyl* **to** *max-cyl* — The seeks occur between these two cylinders.

Subtest 400, Restore Sectors From Service Processor Disk to SMD

copy_f[**rom_spu**] [*filename*]

This command restores sectors previously stored to the service processor disk by the *copy_to_spu* command. If a filename is not specified, the default file created by *copy_to_spu* (filename */mnt/usr/backup_maps/save.s* where *s* is the serial number) is used. This is the file that *copy_from_spu* attempts to read if a file is not specified.

Since the service processor file is in an editable (ASCII) format, the data or the cylinder, head, and sector where it is to be restored can be edited before performing the *copy_from_spu* operation.

Subtest 400, Write Sectors From SMD to Service Processor Disk

copy_t[**o_spu**] [*filename*] *cyl hd sec* [**to** *cyl hd sec*]

This command allows the saving of one or more sectors to the service processor disk in an editable (ASCII) format.

The *copy_from_spu* command restores these sectors. If a filename is not specified, the default file (filename */mnt/usr/backup_maps/save.s* where *s* is the drive's serial number) is used. The save file can be edited to change the data in the sectors or to change where the sectors will be restored. If a file is chosen that already exists, this command overwrites the file.

Arguments:

- *cyl hd sec* — Starting sector
- [**to** *cyl hd sec*] — Ending sector, default is starting sector

Subtest 400, Write Once then Repetitively Read and Verify

da[**ta_verify**] [*nnn* **times**] *cyl hd sec* [**to** *cyl hd sec*] [**with** *pattern*]

This command writes to all the sectors specified with the first default pattern or the pattern specified on the command line. It then rereads the data *nnn* times (or one time by default) without data compare. Only errors detected by the drive or controller are reported. In the list of arguments, [**to** *cyl hd sec*] may be substituted with [**to end**].

Arguments:

- [*nnn* **times**]— Repetition count. Possible values include:
  - **1** — Lower bound value, default value
  - **2,147,483,647** — Upper bound value
- *cyl hd sec* — Starting sector
- [**to** *cyl hd sec*] — Ending sector, default is starting sector
- [**with** *pattern*] — The *pattern* is a 1 to 8 hexadecimal digit pattern

Subtest 400, Select Drive

dr[**ive_select**] [*drive-number*]

This command can change which drive is the active drive. Most of the other interactive test commands operate on the active drive only. The argument *drive-number* is the entry number from the *Drive Configuration Data* which is displayed during the test parameter entry. To redisplay the entry numbers enter **d** and press RETURN. The *Drive Configuration Data* is redisplayed along with which drive is currently active. Then a new drive selection prompt is displayed, and an entry number can be entered to change the active drive or pressing RETURN leaves it unchanged.

Argument:

- [*drive-number*] — The entry number from the *Drive Configuration Data* which is displayed during the test parameter entry, the active drive

The following is an example of displaying the drive configuration data and selecting a drive:

Figure dev5130–23, Displaying Drive Data and Selecting a Drive

```
(D1;save)-> d

                        DRIVE CONFIGURATION DATA
      CCU VME Cntlr Int Unit #   # Phys Log Prev
Drive  #   #   CSR Level #  Cyl Hds Sec Sec Fmtd Name          Serial #
----- --- --- ----- --- --- --- --- --- --- --- ------- ----------------------
   1   3   0  0xc00  1   0  760  19  60  59 yes DKD-206 03991
   2   3   0  0xa00  4   0  760  19  60  59 yes DKD-206 03268
   3   6   1  0xc00  3   0  842  20  46  45 yes DKD-208 04123

        Drive 1 is currently selected
        Enter new selection or 0 to leave it as is (0,1-3) [0] -> 2
        Drive 2 is now selected
(D2;save)-> d 3
        Drive 3 is now selected
(D3;save)->
```

The configuration data is not displayed if the drive number is entered with the command. Also, the previous figure shows that the drive number is redisplayed with each prompt as **D***x* where *x* is the current drive number.

Subtest 400, Dump Defect Lists to Service Processor Disk

du[mp_lists] [**b**][**m**|**g**|**a**]

This command is used to create a backup of the defect lists for the following reasons:

- Before moving a drive to a controller other than the Interphase 4200 SMD controller
- Whenever the disk is going to be completely overwritten for security reasons

The file can be dumped in ASCII or binary. An ASCII file is essential if the purpose is to move the drive to a Multibus system since the Multibus drive formatter can only read ASCII files to date. The binary dump capability is primarily for future use to allow a dump of the defect lists so the lists can be restored with no changes. When restoring an ASCII file, all entries become grown entries which means the information is lost as to whether the flaw originated with the manufacturer or later appeared as a grown defect. Also, a binary dump potentially occupies less room on the service processor disk.

Arguments:

- [**b**] — Dump file in binary (if not specified, dump file in ASCII)
- [**m**] — Dump only Manufacturer's Defects
- [**g**] — Dump only Grown Defects
- [**a**] — Dump all defects, default value

Subtest 400, Reformat One Track

fo[rmat] *cyl hd*

This command is used to unslip sectors, unmap a track, or recreate a bad track's headers. If automatic save is enabled (the prompt indicates *Save*), then before the track is reformatted, an attempt is made to read every logical sector (including relocated sectors). If a read fails, the options of retrying the sector, terminating the format before any destructive operation occurs, or forcing the format even though one or more sectors may not be recovered are given.

> **CAUTION**
>
> If auto-saving is disabled (*Nosave* mode) using the *toggle_save* command, the track is reformatted without preserving the track's data.

Arguments:

- *cyl hd* — Track to reformat

In the following figure, cylinder 300, head 15 is reformatted on an NEC drive (760 cylinders, 19 heads, 59 logical sectors). The track contains one slipped sector.

Figure dev5130–24, Restoring Track Data

```
(D3;Save)-> format 300 15
        No data has been previously saved. Saving this track
        Data save operation complete

 TRACK HEADERS BEFORE FORMAT:
48 49 50 51 52 53 54 55 56 57 58  0  1  2  3 *B  4  5  6  7  8  9 10 11 12
13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
38 39 40 41 42 43 44 45 46 47

        About to format cylinder 300  head 15.
        Flawed sectors associated with this track:
            Manufacturer's Defect list: 4
                These flaws will be reapplied to the track since this list is
                not ignored. To ignore manufacturer's defects, you must
                reformat the drive and change format options.
            Grown Defect list:          none
        Format complete.
        Restoring data to track
        Data restore operation complete

(D3;Save)-> track 300 15
 cylinder = 300  head = 15
 48 49 50 51 52 53 54 55 56 57 58  0  1  2  3 *B  4  5  6  7  8  9 10 11 12
 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
 45 46 47 48 49 50 51 52 53 54
(D3;Save)->
```

CAUTION

If auto-save is enabled and sectors are unslipped by the *format* command, data is restored to the bad sectors which could cause the data to be no longer readable. This is okay since the data is still saved. Slip the bad sectors using the *slip_sectors* command and then use the *restore_track_data* command to restore the track's data again. Also before the reformat, a prompt is displayed to enter which of the grown defects to reslip which allows the reslip to be performed in the same operation.

NOTE

If Manufacturer's Defects have been slipped on a track that is to be reformatted, the defects are reslipped automatically after the format. The only way to unslip Manufacturer's Defects is to reformat the whole disk and specify at format setup time (Subtest 300, Format Setup) that the Manufacturer's Defects are to be ignored by using the *format_options* command.

The following is another example where the entire track has been previously mapped to an alternate track because there were two grown defects (sectors 2 and 3) on the track and only one spare sector was available. The alternate track that was used is cylinder 757 head 13.

Figure dev5130–25, Restoring Data After Testing and Slipping Tracks

```
(D3;Save)-> format 422  1
         No data has been previously saved. Saving this track
         Data save operation complete

  TRACK HEADERS BEFORE FORMAT:
 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13
 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13
 13 13 13 13 13 13 13 13 13

         About to format cylinder 422  head  1.
         Flawed sectors associated with this track:
             Manufacturer's Defect list: none
             Grown Defect list:          2 3
             Enter sectors from GD list you want reslipped
               separated by spaces: 2
          Track is currently mapped to cyl 757 hd 13.
          Do you want this alternate to be marked unusable [yn] (n) -> y
          Format complete.
          Restoring data to track
          Data restore operation complete

(D3;Save)-> track 422  1
 cylinder = 422  head =  1
 55 56 57 58  0  1 *B  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19
 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 45 46 47 48 49 50 51
 52 53 54 48 49 50 51 52 53 54
(D3;Save)->
```

When the format is complete, the only sector still bad is sector 2 and the track is no longer mapped to an alternate track.

Subtest 400, Display Header, Data and ECC

hd[e_display] *cyl hd sec* [**to** *cyl hd sec*]

This command displays the sector data and the header and Error Correction Code (ECC). The data is read in raw mode which means the controller does not perform error checking of the data, so an ECC error is not displayed while performing this operation.

Arguments:

- *cyl hd sec* — Starting sector.
- [**to** *cyl hd sec*]— Ending sector, default is starting sector.

> **NOTE**
>
> The sector specified for the *hde_display* command is the physical sector numbered from index. All other commands search all headers on the track until the header is found.

To illustrate how the *hde_display* command works, the track headers displayed by the *track* command and the sector displayed by the *hde_display* command are shown in the following figure:

Figure dev5130–26, Displaying the Track Headers

```
(D2;Save)-> track 27 5
 cylinder =  27  head =  5
 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 *S  0
  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
 26 27 28 29 30 31 32 33 34 35

(D2;Save)-> hde 27 5 0

Phys:  27  5   0  Log:  27  5  36       Header:a81b0524 05240000 ECC:2bc18e26
000  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
020  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
040  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
060  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
080  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0a0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0c0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0e0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
100  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
120  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
140  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
160  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
180  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1a0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1c0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1e0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6

(D2;Save)->
```

The previous figure shows that the physical sector 0 corresponds to logical sector 36 on this track.

The following figure shows the result of an attempt to display header, data, and ECC for track that has been mapped to an alternate track:

Figure dev5130–27, Displaying a Mapped Track

```
(D2;Save)-> track 286 5
 cylinder = 286  head =  5
 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12
 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12
 12 12 12 12 12 12 12 12 12

(D2;Save)-> hde 286 5 0

Phys: 286  5   0  Log: TRK MAPPED to  757 12     Header:d11e0512 02f50000
```

The following figure shows the result of an attempt to display header, data, and ECC of an alternate track. Specifically, the figure shows the header display (*hde*) of cylinder 757 head 12 physical sector 0 from the previous figure where cylinder 286 head 5 has been mapped to cylinder 757 head 12 physical sector 0.

Figure dev5130–28, Displaying an Alternate Track

```
(D2;Save)-> track 757 12
 cylinder = 757  head = 12
 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 *S  0
  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
 26 27 28 29 30 31 32 33 34 35

(D2;Save)-> hde 757 12 0

Phys: 757 12   0  Log: 286  5  36       Header:a91e0524 05240000
                       This appears to be an alternate track
```

Subtest 400, Display List of Commands and Arguments

h[elp]

This command lists the commands and their arguments.

Subtest 400, List Flaws

l[ist] [m|g|a]

This command lists flaws which have been fixed on the drive. The types of flaws to be listed can be selected as follows:

- [**m**] — List Manufacturer's Defects entries only
- [**g**] — List Grown Defects entries only
- [**a**] — List Manufacturer's Defects and Grown Defects entries, default value

Figure dev5130–29, Example of the List Command

```
format setup (D1;Sector)-> list

Summary of flaws on drive 1 serial number 003013
 CYL HD SEC   BCAI   LEN TYPE  ERR SRC | CYL HD SEC   BCAI   LEN TYPE  ERR  SRC
  17  7  23  35032  4825      NONE USR | 237  0   1   4816    17  MAP  HNF  MAP
 237  0   0   4802   105  MAP HARD MAP |
```

The listing above is double-columned and shows the location of all known flaws for this drive. The fields in each entry have the following meanings:

CYL HD SEC	The cylinder, head and sector impacted by the flaw
BCAI	Byte count after index to the start of the flaw
LEN	Length of the flaw in bits
TYPE	MAP or blank. If MAP, the entire track has been mapped to an alternate track
ERR	The actual error that was detected during pattern test:

Table dev5130–13, Pattern Test Flaws

POSSIBLE VALUES	ERROR CODE	MEANING
CSUM	0x19	Header checksum error
HPAD	0x22	Invalid header pad
SOFT	0x13	Soft ECC error
HARD	0x23	Hard ECC error
HNF	0x29	Sector not found
SYNC	0x2b	Invalid sync in data field
JHDR	0x6a	Unrecognized header field
MHDR	0x6b	Mapped header error
MISC		Any other error
NONE		No error detected during pattern test

SRC Where error originated from:

Table dev5130–14, Sources of Flaws

POSSIBLE VALUES	MEANING
MAP	Came from original Manufacturer's Defect Map
PGM	Discovered during pattern test (Subtest 301)
USR	User input this flaw

Subtest 400, Pattern Test Range of Sectors

p[attern test] [*nnn* **times**] *cyl hd sec* [**to** *cyl hd sec*] [**with** *pat1* [*pat2* ...]]

This command allows the pattern test of selected sectors repetitively. It is useful to check part or all of a system portion of a disk (all cylinders before the diagnostic cylinder and relocated sectors). If the test is constrained to one track, the data is automatically saved and restored when the test is completed. If more than one track is selected, a warning prompt is displayed and the operation can be terminated at this point to prevent permanent overwrite of data. The automatic save can be disabled with the *toggle_save* command. Up to 15 patterns can be specified. In the list of arguments, [**to** *cyl hd sec*] may be substituted with [**to** *end*].

Arguments:

- [*nnn* **times**]— Repetition count. Possible responses include:
  - **1** — Lower bound value, default value.
  - **2,147,483,647** — Upper bound value.
- *cyl hd sec* — Starting sector.
- [**to** *cyl hd sec*]— Ending sector, default is starting sector.
- [**with** *pat1* [*pat2* ...]] — Up to 15 1-8 digit hex patterns can be specified, default is the patterns specified in Subtest 301, Format and Pattern Test or the patterns in the file *dev5130.patt* if this file exists.

The following figure shows the use of the pattern test command:

Figure dev5130–30, Example of Pattern Test Command

```
(D3;Save)-> patt 10 times 0 0 0 to 1 0 0 with 00000000 ffffffff
     Patterns used: 00000000 ffffffff
```

Subtest 400, Enable or Disable Write Protection

pr[otection] [**on** | **off**]

This command enables or disables writes to protected areas.

CAUTION

This command should be used with caution. If protection is turned off, writes can be made anywhere on the disk and can destroy unrecoverable information. If protection is on, writes are only allowed to the alternate track area or the used tracks of the defect cylinder.

On ESDI drives, write are also not allowed to the innermost cylinder which contains the original Manufacturer's Defect map.

Subtest 400, Exit Interactive Test

q[uit]

This command is used to exit the interactive test.

Subtest 400, Restore Previously Saved Track Data

r[estore_track_data]

This command can restore data from the general buffer to the track it was originally read from. The *save_track_data* command stores data into the general buffer from a selected track. In addition, the *format*, *data_verify*, and *pattern_test* commands save into the general buffer before their operation and automatically restore the data afterward. The data remains in the buffer so it can be restored again at a later time if, for instance, the first restore is bad.

If data is saved and is not restored and then an attempt is made to *quit* the interactive test, a message is displayed indicating that there is saved data and a prompt is displayed that allows reentering or exiting the interactive test.

The following figure shows an example of using the restore command:

Figure dev5130–31, Restoring Track Data

```
(D3;Save)-> restore
        Data has been saved for drive 3: cylinder 273  head 17
        Do you really want to restore this data? [yn] -> y
        Data restore operation complete
(D3;Save)->
```

If data is not restored, the operation is terminated and the interactive prompt is displayed.

If the current drive has been changed from drive 3 to drive 9 since the last save operation and the restore command is used, the following is displayed:

Figure dev5130–32, Changing Drives After a Save Operation

```
(D9;Save)-> restore
        Data has been saved for drive 3: cylinder 273  head 17
        However, drive 9 is currently selected.
        Use 'd[rive_select]' to change drives and try again.
(D9;Save)->
```

If data has not been saved before attempting to restore the data, the following is displayed:

Figure dev5130–33, Attempting to Restore Data Before Saving

```
        No data has been previously saved so restore aborted.
(D9;Save)->
```

Subtest 400, Save One Track of Data

sa[ve_track_data] *cyl hd*

This command saves one track of data into the general buffer. The data can be restored with the *restore_track_data* command. Data on relocated sectors is also saved so if a track is reformatted (which removes the relocated sectors) all the track's data can still be restored.

Arguments:

- *cyl hd* — Track to be saved

The following is an example of saving one track:

Figure dev5130–34, Saving One Track

```
(D4;Nosave)-> save 525 5
        Data has already been saved for drive 4: cyl=601, hd=14
        Are you sure you want to overwrite this data? [yn] -> y
        Data save operation complete
(D4;Nosave)->
```

The prompt in the previous figure specifies *Nosave* which indicates that the command *toggle_save* was previously entered so that saves are not automatic on destructive operations. But, *Nosave*

does not effect this command. Normally, *Save* is displayed since disabling automatic save can cause loss of data.

Subtest 400, Display Data From Range of Sectors

sec[tor_display] *cyl hd sec* [**to** *cyl hd sec*]

This command displays the data from one or more consecutive sectors.

Arguments:

- *cyl hd sec* — Starting sector.
- [**to** *cyl hd sec*] — Ending sector, default is starting sector.

The following is an example of using the *Sector_display command*:

Figure dev5130–35, Displaying Sector Data

```
(D1;Save)-> sector 27 5 55

        Sector  27  5 55:
000  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
020  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
040  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
060  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
080  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0a0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0c0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
0e0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
100  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
120  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
140  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
160  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
180  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1a0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1c0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6
1e0  6db66db6 6db66db6 6db66db6 6db66db6  6db66db6 6db66db6 6db66db6 6db66db6

(D1;Save)->
```

The previous example is almost identical to the one for the ***hde_display*** command. The major difference between the two commands is that with the ***sector_display*** command, the read is sensitive to data errors. In the raw read mode that ***hde_display*** uses, no data errors are reported. If a data error does occur while executing the ***sector_display*** command, then an error message is displayed, and a prompt is displayed to retry, force, or skip the read.

If a retry of the read is specified, the number of read attempts to try before displaying another error message can be specified. From 1 to 2,147,483,647 retries can be specified. Every five retries a seek is alternately performed one cylinder in and back or one cylinder out and back. Any successful read terminates the retries and the data is displayed.

If a force of the error is specified, one more read is performed with a *move bad data* indication to the controller. Whatever is read on this attempt is displayed. An error indication is not displayed if an error occurs on this read.

If a fix of the error is specified, Error Correction Code (ECC) correction is applied if the error is correctable.

If *skip* is specified, the sector is skipped. If there are any more sectors to read in the range specified, then the display of data continues with the next sector.

The following is an example of a read that fails:

Figure dev5130–36, Failed Read Example

```
(D1;Save)-> sector 400 22 18 to 400 22 19

dev5130 drv 1 ERROR 1e(cntlr) Soft ECC Error
 cyl:400 hd:22 sec:18

                        1 attempts to read sector failed
                        what to do [# of retries/force/skip/fix] (1) -> 100

dev5130 drv 1 ERROR 1e(cntlr) Soft ECC Error
 cyl:400 hd:22 sec:18

                        100 attempts to read sector failed
                        what to do [# of retries/force/skip/fix] (100) -> skip


       Sector 400 22 19
000  00000000 00000000 00000000 ff300020  1023eee10 99903220 b2d3d4d1 ab222290
020                     ---------------- etc ----------------
```

In the previous figure sector 18 is not displayed since it was skipped. What is displayed is the next sector, sector 19 which was read successfully on the first attempt. If `fix` had been specified for sector 18, it would have been displayed since soft ECC errors were occurring which are correctable.

Subtest 400, Display or Change Disk Serial Number

ser[ial_number] [*number*]

This command displays the drive's serial number. To change the serial number, follow the command with the new serial number.

Subtest 400, Slip One or More Sectors

sl[ip_sectors]

This command is used to slip sectors or map tracks which are generating errors or to enter defect map information to slip sectors. If track data is automatically saved (indicated by the word *Save* in the prompt), an attempt to save and restore all affected tracks is made to minimize data loss unless automatic save is disabled with the *toggle_save* command.

NOTE

When entering the defect map for a new disk, a disk that has just been formatted and does not yet contain a file system, the automatic save may be disabled with the *toggle_save* command before entering the *slip_sectors* command. This causes the slip to proceed much faster.

CAUTION

If any usable data exists on these tracks, the data is lost.

The *slip_sectors* command starts up a separate command processor which expects bad sectors or defect map information to be entered. There is a help facility which lists the available commands if **h** is entered. The help screen is shown as follows:

Figure dev5130–37, *Slip_Sectors* Help Screen

```
SLIP_SECTORS commands:
q[uit]                          - exit from 'slip_sectors'
c[hange_mode]                   - toggles logical sector/defect
                                  map entry mode
cyl hd sec                      - logical sector to be slipped
cyl hd bcai len                 - defect map entry to be slipped
de[lete] cyl hd sec             - delete logical sector entry
de[lete] cyl hd bcai len        - delete defect map entry
e[xecute]                       - slip the sectors now
f[ile] filename                 - get inputs from specified file
h[elp]                          - display this information
l[ist]  [m|g|a|n]               - list inputs made so far
m[ap_track] cyl hd              - map track to an alternate
!unix-command                   - execute unix command
'comment                        - comment; ignored
```

To slip sectors which are generating errors, the normal usage is to enter all sectors which need to be slipped, verify the entries using the *list* command, delete any incorrect entries with the *delete* command, and then begin the slipping with the command *execute*. New sectors can be entered at any time up until the *execute* command is entered. As a safeguard, when the *execute* command is typed, the list of sectors is automatically displayed and a prompt is displayed to confirm the list. By replying **n** to the confirmation, the *slip_sectors* prompt is displayed with all inputs still intact.

slip_sectors' change_mode Command

c[hange_mode]

The *change_mode* command is used to toggle between the logical sector and defect map entry

mode. The current input mode (logical sector or defect map mode) is revealed in the slip prompt as shown in the following figure:

Figure dev5130–38, Changing Entry Modes

```
slip (D1;Save;Sector)->c
slip (D1;Save;Defect)->
```

slip_sectors' cyl hd sec and *cyl hd bcai len* Commands

cyl hd sec

or:

cyl hd bcai len

These commands are used to enter the logical sector to be slipped or to enter the defect map entry to be slipped. When a defect is entered, the associated track's headers are listed as shown in the following figure:

Figure dev5130–39, Entering a Defect

```
slip (D1;Save;Defect)-> 293 1 572 9510
        Associated logical sectors: 55 56 57
```

The previous figure illustrates that three sectors are affected by the media flaw which starts at byte 572 from index and is 9510 bits long.

If two defects exist that affect the same sector, the logical sector is only entered in the list of flaws once. Subsequent entries of the same sector are ignored and an appropriate warning is displayed.

For instance, if the following two defects exist:

cylinder	head	bcai	bit-length
10	0	70	1
10	0	80	1

Both defects fall in sector 0 so when the second defect is entered, it is not slipped again. The slipping of sectors with two defects is shown in the following figure:

Figure dev5130–40, Slipping Sectors With Two Defects

```
slip (D1;Save;Defect)-> 10 0 70 1
       Associated logical sectors: 0
slip (D1;Save;Defect)-> 10 0 80 1
                    Cyl 10 Hd 0 Sec 0 already exists. Duplicate entry not created.
slip (D1;Save;Defect)-> list

Summary of new flaws on drive 1 serial number 02039
 CYL HD SEC   BCAI   LEN TYPE  ERR SRC | CYL HD SEC   BCAI   LEN TYPE  ERR SRC
  10  0   0     70     1      NONE NEW |
```

NOTE

In the current version of *dev5130*, no bytes are considered part of a gap. A flaw in any byte *results* in one or more sectors being slipped.

slip_sectors' delete Command

de[lete] *cyl hd sec*

or:

de[lete] *cyl hd bcai len*

The *delete* commands listed above are used to delete logical sector entries or to delete defect map entries. The following figure shows how to delete bad inputs. The *list* command is used after the *delete* command to verify that the bad inputs were deleted.

Figure dev5130–41, Deleting Bad Inputs

```
(D1;Save)-> slip
Type 'h' for help with slip commands
slip (D1;Save;Sector)-> 17 7 23
slip (D1;Save;Sector)-> 17 7 46
slip (D1;Save;Sector)-> d 17 7 46
       Sector  17  7 46 has been removed from the inputs
slip (D1;Save;Sector)-> list

Summary of new flaws on drive 1 serial number 02039
 CYL HD SEC   BCAI   LEN TYPE  ERR SRC | CYL HD SEC   BCAI   LEN TYPE  ERR SRC
  17  7  23                   NONE USR |
```

slip_sectors' execute Command

e[xecute]

The *execute* command is used slip the sectors specified. When the slip is executed, the sectors are slipped one track at a time or the track is mapped if not enough spare sectors exist. If automatic save is active, the data for the track is copied to a special buffer (not the general buffer used by *save_track_data*) before the slip and is restored after the slip.

To verify the slip, display the track headers once more using the *track_headers_display* command. All slipped sectors are marked with a **B*. Mapped tracks have the same number for all sectors. This number is the head number of the alternate track. An example of displaying the track headers after slipping sector 255 0 6 is shown in the following figure:

Figure dev5130–42, Display Slipped Track Headers

```
(D1;Save)-> track 255 0
cylinder = 255  head =  0
 0  1  2  3  4  5 *B  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48
49 50 51 52 53 54 55 56 57 58
```

If defect input mode is activated and an attempt is made to slip the sector on track 255 head 0 which has already been marked bad in the previous figure, the following figure shows what would be displayed:

Figure dev5130–43, Slipped Tracks Previously Marked Bad

```
slip (D1;Save;Defect)-> 255 0 3800 1
        Cyl 255 Hd 0 Sec 6 already exists. Duplicate entry not created.
```

slip_sectors' file Command

f[ile] *filename*

The file command is used to get inputs from a specified file. To input defects from a file, first create the file as documented in Subtest 300, Format Setup. Then type the command **file** *filename* where *filename* represents the actual filename. The defects in this file can be in byte-count-after-index or logical sector format. The file can also contain track entries which specify tracks to be mapped to alternate tracks.

slip_sectors' help Command

h[elp]

This command lists the commands and their arguments.

slip_sectors' list Command

l[ist] [**m**|**g**|**a**|**n**]

This command lists flaws which have been fixed on the drive. The types of flaws to be listed can be selected as follows:

- [**m**] — List Manufacturer's Defects entries only
- [**g**] — List Grown Defects entries only
- [**a**] — List Manufacturer's Defects and Grown Defects entries, default value
- [**n**] — List defect needs

slip_sectors' map_track Command

m[ap_track] *cyl hd*

To map an entire bad track, use the *map_track cyl hd* command. The test selects one of the alternate tracks for use. If data is being saved, then the original track's data is restored to the alternate track.

slip_sectors' quit Command

q[uit]

To exit the *slip_sectors* command at any time enter the *quit* command.

slip_sectors' Execute UNIX Command

!*UNIX-command*

This command is used to issue UNIX commands. After the UNIX command is completed, execution is returned to the interactive prompt. UNIX commands can be issued from any prompt throughout the test.

slip_sectors' Enter Comments

'*comment*

This command is used to enter a comment. To enter a comment, type the ' command and a comment. The comment is echoed so it is redirected output. This is useful to document redirected output.

slip_sectors Command Examples

The following figure contains examples of several *slip_sectors* commands.

Figure dev5130–44, Command Examples

```
slip (D1;Save;Sector)-> 17 7 36
slip (D1;Save;Sector)-> 247 12 4
slip (D1;Save;Sector)-> 256 0 12
slip (D1;Save;Sector)-> d 256 0 12
slip (D1;Save;Sector)-> 255 0 12
slip (D1;Save;Sector)-> list

Summary of new flaws on drive 1 serial number 02039
 CYL HD SEC   BCAI   LEN TYPE  ERR SRC | CYL HD SEC   BCAI   LEN TYPE  ERR SRC
  17  7  23  35032  4825  MAP NONE USR | 247 12   4   2432  4825      NONE USR
  17  7  36   6644  4825  MAP NONE USR | 255  0  12   7904  4825  MAP NONE USR

slip (D1;Save;Sector)-> e

Summary of new flaws on drive 1 serial number 02039
 CYL HD SEC   BCAI   LEN TYPE  ERR SRC | CYL HD SEC   BCAI   LEN TYPE  ERR SRC
  17  7  23                  NONE USR | 247 12   4                   NONE USR
  17  7  36                  NONE USR | 255  0  12                   NONE USR

       Are you sure inputs are ready for slipping? [yn] -> y

Number of spares per track: 1
 cyl hd sec  bcai  len  action              additional information
---- -- --- ----- ----- ------- ---------------------------------------------
  17  7  23 35032  4825 mapped  Alternate track used: cylinder 757 head 13
  17  7  36  6644  4825 mapped  Alternate track used: cylinder 757 head 13
 247 12   4  2432  4825

dev5130 drv 1 ERROR 23(cntlr) Hard ECC error
 cyl:247 hd:12 sec:4

                      1 attempts to read sector failed
                      what to do [# of retries/force/skip/fix] (1) -> fix
Number of spares per track: 1
 cyl hd sec  bcai  len  action              additional information
---- -- --- ----- ----- ------- ---------------------------------------------
 247 12   4  2432  4825 slipped
 255  0  12  7904  4825 mapped  Alternate track used: cylinder 757 head 12

slip (D1;Save;Sector)-> q
```

In the previous figure, the *cyl hd sec*, *delete*, *list*, *execute*, and the *quit* commands are displayed. Sector 247 12 4 is difficult to read (hard ECC error). After the first attempt fails, a request is made to fix the error. The next attempt has either a soft Error Correction Code (ECC) error or no error is reported. If an error is not fixable, specifying *force* results in one more read of the sector with the controller set to move bad data. If *skip* is selected, the remaining slips are still performed. Retries are allowed by entering the number of retries or by pressing RETURN to use the default number of retries. Every five retries a seek is alternately performed one cylinder in and

back or one cylinder out and back.

In the following figure the track headers are displayed again to verify the slips:

Figure dev5130–45, Displaying the Track Headers

```
(D1;Save)-> track 17 7
cylinder =  17  head =  7
 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13
 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13 13
 13 13 13 13 13 13 13 13 13 13

(D1;Save)-> track 247 12
cylinder = 247  head = 12
  0  1  2  3 *B  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48
 49 50 51 52 53 54 55 56 57 58

(D1;Save)-> track 255 0
cylinder = 255  head =  0
 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12
 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12 12
 12 12 12 12 12 12 12 12 12 12
```

In the previous figure Track 17 7 and track 255 0 have been relocated to head 13 and head 12 respectively of the relocation area. The cylinder is not known but can be determined by using the *hde_display* command on any sector of the bad track. Track 247 12 has one bad sector and no spare sector.

In the following figure all flaws are redisplayed to verify the relocation actually occurred:

Figure dev5130–46, Display All Flaws to Verify Relocation

```
(D1;Save)-> list

BAD BLOCK TABLE FOR ccu/mb/csr/d=3/0/3f0/0

Summary of new flaws on drive 1 serial number 02039
 CYL HD SEC   BCAI   LEN TYPE  ERR SRC | CYL HD SEC   BCAI   LEN TYPE  ERR SRC
  17  7  23  35032  4825  MAP NONE USR | 247 12   4   2432  4825       NONE USR
  17  7  36   6644  4825  MAP NONE USR | 255  0  12   7904  4825  MAP NONE USR

(D1;Save)->
```

If there had already been entries in the table, they would have been displayed in the previous figure also. This list of the flaws actually comes from a copy of the table kept in main memory. However, it does reflect what is on the disk since both the *slip_sectors* and *format* commands

rewrite all five copies of the defect lists before returning to the interactive prompt. To reread them off the disk before listing them, use the *status* command. It rereads all lists before displaying the status of the lists.

One other verification to perform is a *verify_format* on each of the tracks.

Subtest 400, Display Information About Device

st[atus]

This command lists the drive configuration data (all selected drives) and displays which drive is the currently active drive. The *Status* command also displays which track was last saved in the general buffer by using one of the commands: *format*, *save_track_data*, *data_verify*, or *pattern_test*. In addition, a line is displayed which indicates whether the automatic save of track data is enabled (*Save* is also shown in the prompt). If the drive is previously formatted, then the following information is also displayed:

a. The status of all copies of defect lists and track logs on the disk.

b. The revision of the formatter that originally formatted the disk.

c. The revision of the formatter that last reformatted the disk.

d. The date the drive was originally formatted.

e. The date the drive was last reformatted.

f. The serial number of the drive.

This information is from the defect list cylinder which is reread each time the *status* command is entered. The following figure shows the information that is displayed when the *status* command is entered:

Figure dev5130–47, Displaying Device Information

```
(D1;Save)-> status

                        DRIVE CONFIGURATION DATA
      CCU VME Cntlr Int Unit #   # Phys Log Prev
Drive  #   #   CSR Level #  Cyl Hds Sec Sec Fmtd Name          Serial #
----- --- --- ----- --- --- --- --- --- --- --- ------- ----------------------
   1   3   0  0xc00  1   0  760  19  60  59 yes DKD-206 03991
   2   3   0  0xa00  4   0  760  19  60  59 yes DKD-206 03268
   3   6   1  0xc00  3   0  842  20  46  45 yes DKD-208 04123

Drive 1 is currently selected
Saved Track:  drive 3  cylinder 300 head 12
Save of track data is automatic during destructive commands.
Status of defect lists:
Drive  1 All copies are GOOD
Drive information
        Serial number: 03991
        Original Formatter Version: 3.00 Date: Mon Mar 14 17:33:24 CST 1988
        Latest Disk Update Version: 3.00 Date: Tue Mar 15 10:23:14 CST 1988
        Format options: Manufacturer's defect list was used if available
                        Pattern test was completed using pattern set 2

(D1;Save)->
```

Subtest 400, Enable and Disable of Automatic Save

to[*ggle_save*]

This command switches between enabling and disabling of automatic save. Automatic save occurs during the commands *format*, *pattern_test*, *data_verify* and *slip_sectors*. The displayed interactive prompt indicates whether automatic save is enabled (Save) or disabled (Nosave). The *Status* command also displays the current setting of automatic save.

Subtest 400, Display Track Headers

tr[**ack_headers_display**] *cyl hd* [**to** *cyl hd*]

This command displays the sector numbers for each of the sectors on a track. The sector number that is displayed first is located physically just after the index so it will not always be zero. This is because sectors may be skewed and interleaved. For a skew of 5, head 0 logical sector 0 is the first sector after index. On head 1, logical sector 0 is the sixth sector, on head 2, logical sector 0 is the eleventh sector and so on.

Arguments:

- *cyl hd* — Starting sector.
- [**to** *cyl hd*] — Ending sector, default is starting sector.

Each track has one spare sector (unless it is used because one or more sectors were slipped on the track). The spare sector is marked *S. If any sectors have been flagged as bad, they are marked *B.

If the entire track has been remapped to an alternate track, then the head number of the alternate track is displayed. To find out what alternate track is being used, use the ***hde_display*** command.

The following figure shows the display of sector numbers for sectors and a ***S** for a spare sector on a track:

Figure dev5130–48, Displaying Sector Numbers and Spare Sector

```
(D1;Save)-> track 427 2
cylinder = 427  head =  2
50 51 52 53 54 55 56 57 58 *S  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14
15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47 48 49
(D1;Save)->
```

In the previous figure, sector 0 is actually the eleventh sector on the track since it is head 2 with a skew of 5. Also the spare sector (*S) is just before sector 0.

The following figure shows the display of sector numbers for sectors and a ***B** for a bad sector on a track:

Figure dev5130–49, Displaying Sector Numbers and Bad Sector

```
(D1;Save)-> track 208 11
cylinder = 208  head = 11

 5 *B  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
54 55 56 57 58  0  1  2  3  4

(D1;Save)->
```

In the previous figure, one sector has been flagged bad and the spare sector has been used. Also sector zero is skewed almost to the end of the track because it is head 11 with a skew of 5.

Subtest 400, Verify a Range of Sectors

v[**erify_format**] [*nnn* **times**] *cyl hd sec* [**to** *cyl hd sec*]

This command performs repeated reads on a range of sectors in an attempt to detect read errors. The command is not data destructive. It does not perform a data compare since the data is unknown. As the ***verify*** is executed, a pass count is incremented on the display to indicate how far the execution has progressed. Any errors are displayed without retry and the reads continue. If any sectors have been relocated, the relocated sectors are read. In the list of arguments, [**to** *cyl hd sec*] may be substituted with [**to end**].

Arguments:

- [*nnn* **times**]— Repetition count. Possible responses include:
  - **1** — Lower bound value, default value
  - **2,147,483,647** — Upper bound value
- *cyl hd sec* — Starting sector
- [**to** *cyl hd sec*]— Ending sector, default is starting sector

Subtest 400, Execute UNIX Command

!*UNIX-command*

This command is used to issue UNIX commands. After the UNIX command is completed, execution is returned to the interactive prompt. UNIX commands can be issued from any prompt throughout the test.

The following figure shows an example of entering the ! command and the UNIX command **ps**:

Figure dev5130–50, Executing UNIX Command From Interactive Test Prompt

```
(D1;Save)-> !ps
   PID TTY TIME CMD
     2 co  0:08 -
   273 co  0:00 dshell
   274 co  0:09 dev5130.t -c 4
   281 co  0:00 sh -c ps?
   282 co  0:02 ps
(D1;Save)->
```

Subtest 400, Enter Comments

'*comment*

This command is used to enter a comment. To enter a comment, type the ' command and a comment. The comment is echoed so it is redirected output. This is useful to document

redirected output.

Examples of Typical Usage of This Test

This section is designed for the casual user who has a general knowledge of disk drives and wants to do some basic operations on disks such as formatting, verifying previously formatted disks, and slipping a sector when the sector is reported bad by CONVEX UNIX. The following examples assume the drives are already cabled up, the VIOP is working, and the switches and jumpers on the controllers and drives are set properly.

Formatting One or More Disks at the Same Time

Up to 12 drives can be formatted at the same time while CONVEX UNIX is not running.

> **WARNING**
>
> CONVEX UNIX cannot be running concurrently with the *dev5130* test.

This example assumes all the drives selected have not been previously formatted. Therefore, the manufacturer's original defect map is read from the drive during Subtest 300, Format Setup. If any of the drives are previously formatted on a CONVEX system with a VME controller, then **y** should be entered to the `Previously formatted` prompt and RETURN should be entered to `Serial number` prompt so the serial number is read from the drive. If an incorrect reply is entered to the `Previously formatted` prompt, the test detects the error in Subtest 300, Format Setup and then the reply can be changed.

> **NOTE**
>
> Previously formatted means that Subtest 300, Format Setup has been completed; not that all of Class 3 subtests have been completed.

The sequence of commands to invoke the formatter are shown in the following figure:

Figure dev5130–51, Formatter Invocation Sequence

```
(spu)> sysreset; mminit -s; dshell RETURN
CONVEX DIAGNOSTIC SHELL
: test dev5130 -c 3 RETURN
```

The following figure shows the prompts and responses to format three drives which have never been formatted before.

Figure dev5130–52, Formatting Three Unformatted Drives

```
                ENTER TEST PARAMETERS
       []     Encloses allowed input ranges or values
       ()     Encloses the default value
       ^      Returns to the previous prompt
       :nn    Returns to the prompt # nn
       :      Returns to the first unsatisfied prompt
       :?     Reviews previous entries
 1:  Use defaults except allow destructive writes [y,n]
                                                (y) -> RETURN

              PERIPHERAL CONFIGURATION DATA
    CCU       Chassis   Type      CSR     Int  Unit  Type
    --------  -------  --------  -----   ---  ----  -------
 1) viop 7       0      DKC-204   0xa00    1    0    DKD-206
 2) viop 7       0      DKC-204   0xc00    4    0    DKD-208
 3) viop 7       1      DKC-203   0xa00    3    0    DKD-214
Enter device 99 to begin user-defined configurations or -1 to end selection
 2:  Device selection [-1,1-3,99]                (-1) -> 1
 3:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                       (n) -> RETURN
 4:  Serial number (5 to 31 characters) []
                          (Default: read from drive) -> 03658
 5:  Device selection [-1,1-3,99]                (-1) -> 2
 6:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                       (n) -> RETURN
 7:  Serial number (5 to 31 characters) []
                          (Default: read from drive) -> 04012
 8:  Device selection [-1,1-3,99]                (-1) -> 3
 9:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                       (n) -> RETURN
10:  Serial number (5 to 31 characters) []
                          (Default: read from drive) -> 14539
11:  Device selection [-1,1-3,99]                (-1) -> RETURN
12:  Enter OK, or :NN to return to question NN [OK]
                                                (OK) -> RETURN

     ------- summary of inputs prints here -------

***********************************************
* DATA DESTRUCTIVE OPERATION IS ABOUT TO START.*
* VERIFY WRITE-PROTECT IS SET ON ALL DRIVES    *
* EXCEPT THOSE YOU ARE TESTING/FORMATTING.     *
***********************************************

Then reconfirm that you want to continue [yn] -> y
```

Figure dev5130–52, Formatting Three Unformatted Drives (continued)

```
        Subtest 300  0:00:00 Prepare for format

Type 'h' for help with commands
format setup (D1;Sector)->continue

                     0:07:50 Reading Manufacturer's Defect Maps
        Preparing cylinder for defect lists on drive(s) 1 2 3
                     0:08:30  passed
        Subtest 301  1:40:00  passed
        Subtest 302  0:00:00  Fix flaws

Summary of all flaws on drive 1 serial number 03658:
 CYL HD SEC  BCAI   LEN TYPE  ERR SRC | CYL HD SEC  BCAI   LEN TYPE  ERR SRC
   ---------- list of all flaws for this drive prints here ----------

Summary of all flaws on drive 2 serial number 04012:
 CYL HD SEC  BCAI   LEN TYPE  ERR SRC | CYL HD SEC  BCAI   LEN TYPE  ERR SRC
   ---------- list of all flaws for this drive prints here ----------

Summary of all flaws on drive 3 serial number 14539:
 CYL HD SEC  BCAI   LEN TYPE  ERR SRC | CYL HD SEC  BCAI   LEN TYPE  ERR SRC
   ---------- list of all flaws for this drive prints here ----------

                     0:03:00  passed
        Subtest 303  0:11:00  passed
        Subtest 304  0:08:00  passed
        Subtest 305  0:00:50  passed
        Subtest 306  0:00:05  passed

************** Test started Wed Mar 16 08:03:52 1988
************** Test ended   Wed Mar 16 10:23:46 1988

test 'dev5130.t' passed
```

Approximate format times for current CONVEX drives are listed in the following table:

Table dev5130–15, Drive Format Times

DRIVE	TIME (hr:min)
NEC 2352 (1/2-GByte)	1:30
NEC 2363 (1-GByte)	2:30
Hitachi 514-38	1:20

If one NEC 2352 and one NEC 2363 are being formatted, the format of the drives will take 2.5 hours plus 5 minutes (5 minutes for each additional drive after the first drive). The NEC 2352 will not finish in 1.5 hours in this case because each subtest must complete on all drives before the next subtest begins. The NEC 2352 will finish each subtest before the NEC 2363 but must wait for the NEC 2363 to complete the subtest.

Subtest 306, Verify Pattern Test Error Threshold will fail if any flaws are found on a drive

during the pattern test which were not in the existing defects lists. This is not normally a significant concern unless several new flaws are occurring. Inspect the list printed during Subtest 302, Fix Flaws and see how many entries are marked PGM instead of USER or MAP.

Verifying the Format of One or More Drives

When a disk or set of disks appear to have read problems, verify that the problem repeats by reading all the usable parts of each disk. Then cables or controllers or drives can be changed to verify the disks again. To verify the usable parts of each disk execute Subtest 304, Verify System Format. This subtest performs a read-only operation to locate any unfixed media flaws or to detect problems with the hardware.

The sequence of commands to invoke Subtest 304, Verify System Format are shown in the following figure:

Figure dev5130–53, Verify Format Invocation Sequence

```
(spu)> sysreset; mminit -s; dshell RETURN

CONVEX DIAGNOSTIC SHELL

: test dev5130 -s 304 RETURN
```

Upon invocation of Subtest 304, the prompts in the following figure are displayed. Reply to the prompts as shown in the following figure:

Figure dev5130–54, Verify Format Parameter Menu

```
                ENTER TEST PARAMETERS
      []     Encloses allowed input ranges or values
      ()     Encloses the default value
      ^      Returns to the previous prompt
      :nn    Returns to the prompt # nn
      :      Returns to the first unsatisfied prompt
      :?     Reviews previous entries
 1:  Use defaults except allow destructive writes [y,n]
                                                  (y) -> n
 2:  Are writes to other than the diagnostics cylinder allowed
    [y,n]                                         (n) -> RETURN
 3:  Are writes to the diagnostics cylinder allowed
    [y,n]                                         (n) -> RETURN
 4:  Number of errors allowed per device each subtest
    [0-65535]                                     (0) -> 100
 5:  Number of devices failed after which test aborts
    [0-65535]                                    (12) -> RETURN
 6:  Threshold for new flaws found during pattern test
    [0-65535]                                     (0) -> RETURN
 7:  Verbosity of test [0-63]                     (3) -> RETURN
 8:  If pattern testing, start after last completed pattern
    [y,n]                                         (y) -> RETURN

              PERIPHERAL CONFIGURATION DATA
     CCU     Chassis   Type      CSR     Int  Unit  Type
    ------  -------  --------  -----  ---  ----  -------
 1) viop 7     0      DKC-204   0xa00   1     0    DKD-206
 2) viop 7     0      DKC-204   0xc00   4     0    DKD-208
 3) viop 7     1      DKC-203   0xa00   3     0    DKD-214

Enter device 99 to begin user-defined configurations or -1 to end selection
 9:  Device selection [-1,1-3,99]                (-1) -> 1
10:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                        (n) -> y
11:  Serial number (5 to 31 characters) []
                          (Default: read from drive) -> RETURN
12:  Device selection [-1,1-3,99]                (-1) -> 2
13:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                        (n) -> y
14:  Serial number (5 to 31 characters) []
                          (Default: read from drive) -> RETURN
15:  Device selection [-1,1-3,99]                (-1) -> 3
16:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                        (n) -> y
17:  Serial number (5 to 31 characters) []
                          (Default: read from drive) -> RETURN
18:  Device selection [-1,1-3,99]                (-1) -> RETURN
19:  Enter OK, or :NN to return to question NN [OK]
                                                (OK) -> RETURN

     ------- summary of inputs prints here -------
```

Figure dev5130–54, Verify Format Parameter Menu (continued)

```
        Subtest 304  0:03:26
dev5130 drv 2 ERROR 13(cntlr) Soft ECC error
  Cyl: 326 Hd: 7 Sect: 12
                     0:05:41
dev5130 drv 3 ERROR 1e(cntlr) Drive faulted
                     0:08:05  passed

************** Test started Wed Mar 16 08:03:52 1988
************** Test ended   Wed Mar 16 10:23:46 1988

test 'dev5130.t' passed
```

In the previous figure, drive 2 appears to have a new defect at cylinder 326 head 7 sector 12. The defect should be verified before slipping the sector. Refer to the next section for information about verifying a defect and slipping a sector. Drive 3 appears to have a more serious problem. The drive faulted in the middle of the subtest. The fault condition is immediately cleared and the operation is retried. The retry succeeded since the drive passed the subtest. This type of error is difficult to isolate. The drive could actually be reporting a fault condition but the problem could also be cabling or a bad controller. Subtest 400, Interactive Test should be used to isolate intermittent problems.

Slipping a Sector

The following example shows how the *dev5130* disk formatter can be used to map out media flaws so those portions of the disk are not used. However, before attempting to slip any sectors which have been reported bad by CONVEX UNIX, consider the following points:

1. Is the error at the reported cylinder, head and sector repeatable? Media flaws usually repeat. This example shows how to confirm a flaw. When confirming the flaw, if *dev5130* prints one of the following error messages, then the error is slippable. Otherwise, some other problem that is not media-related is causing the error.

   The following table lists the media-related errors (use code to correlate with UNIX-reported error):

Table dev5130–16, Media-Related Errors

ERROR CODE	ERROR DESCRIPTION
0x13	Soft ECC error
0x19	Header checksum error
0x22	Invalid header pad
0x23	Hard ECC error
0x29	Sector not found
0x2b	Invalid sync in data field
0x31	Invalid sync in header
0x6a	Unrecognized header field
0x6b	Mapped header error

2. The Manufacturer's Defect map is used on all drives when they are formatted. In the past, the map has proven to be reliable in identifying media flaws. Therefore, any new flaws indicate possible drive unreliability. If a drive has new defects, the media may be degrading. Slip the first one or two new defects but if new defects continue, a new drive should be installed.

In the following example, CONVEX UNIX has been reporting a soft Error Correction Code (ECC) error at cylinder 356 head 1 sector 19 on drive 1, an NEC 2352 1/2-GByte drive. An inspection of the file */mnt/errlog* on the service processor indicates the error has occurred three times always at the same location. The system has been brought down to the service processor and *dev5130* is about to be executed. The goal is to perform the following:

1. Check the status of the drive to see if it has had maintenance since it was originally formatted.
2. Verify the error is real and is at the same location. Also, see if old errors are located on the same surface near this flaw. For instance, the cylinder number differs by one or two from a previous error, but the head and sector are the same. This condition is an excellent indicator that a real error exists and the media flaw is impacting more than one track on a surface.
3. Slip the bad sector(s).
4. Verify the entire disk to see if any other grown errors occur.

First, invoke the interactive test as shown in the following figure:

Figure dev5130–55, Interactive Test Invocation Sequence

```
(spu)> sysreset; mminit -s; dshell RETURN
CONVEX DIAGNOSTIC SHELL
: test dev5130 -c 4 RETURN
```

Upon invocation of the Class 4 subtest, the prompts in the following figure are displayed. Reply to the prompts as shown in the following figure:

Figure dev5130–56, Interactive Test Parameter Menu

```
                ENTER TEST PARAMETERS
       []     Encloses allowed input ranges or values
       ()     Encloses the default value
       ^      Returns to the previous prompt
       :nn    Returns to the prompt # nn
       :      Returns to the first unsatisfied prompt
       :?     Reviews previous entries
 1:  Use defaults except allow destructive writes [y,n]
                                                 (y) -> y

                PERIPHERAL CONFIGURATION DATA
    CCU     Chassis   Type      CSR     Int  Unit  Type
   ------   -------  --------  -----   ---  ----  -------
 1) viop 7     0      DKC-204   0xa00    1     0    DKD-206
 2) viop 7     0      DKC-204   0xc00    4     0    DKD-208
 3) viop 7     1      DKC-203   0xa00    3     0    DKD-214
Enter device 99 to begin user-defined configurations or -1 to end selection
 2:  Device selection [-1,1-3,99]                (-1) -> 1
 3:  Previously formatted on CONVEX system with Interphase 4200/4201 controller
     [y,n]                                        (n) -> y
 4:  Serial number (5 to 31 characters) []
                          (Default: read from drive) -> RETURN
 5:  Device selection [-1,1-3,99]                (-1) -> RETURN
 6:  Enter OK, or :NN to return to question NN [OK]
                                                 (OK) -> RETURN

     ------- summary of inputs prints here -------

**********************************************
* DATA DESTRUCTIVE OPERATION IS ABOUT TO START.*
* VERIFY WRITE-PROTECT IS SET ON ALL DRIVES    *
* EXCEPT THOSE YOU ARE TESTING/FORMATTING.     *
**********************************************

Then reconfirm that you want to continue [yn] -> y

        Subtest 400  0:00:00 Interactive test
Reading defect lists from all selected drives...
Drive  1 All copies are GOOD

                        INTERACTIVE TEST MODE
                        FOR SMD AND ESDI DRIVES

Type 'h' for help
(D1;Save)->
```

Once the `(D1;Save)->` prompt is displayed, any interactive command can be entered.

STEP 1: First check the status of the drive.

In the following figure, the *status* command is entered to display the status of the drive.

Figure dev5130–57, Use of Status Command Example

```
(D1;save)-> status

                        DRIVE CONFIGURATION DATA
      CCU VME Cntlr Int Unit #   # Phys Log Prev
Drive  #   #   CSR Level #  Cyl Hds Sec Sec Fmtd Name          Serial #
----- --- --- ----- --- --- --- --- --- --- --- ------- ----------------------
   1   7   0  0xa00  1   0  760  19  60  59 yes DKD-206 03658

Drive 1 is currently selected
No track data has been saved yet.
Save of track data is automatic during destructive commands.
Status of defect lists:
Drive  1 All copies are GOOD
Drive information
        Serial number: 03658
        Original Formatter Version: 3.00 Date: Mon Mar 14 17:33:24 CST 1988
        Latest Disk Update Version: 3.00 Date: Wed May 11 14:03:14 CST 1988
        Format options: Manufacturer's defect list was used if available
                        Pattern test was completed using pattern set 2

(D1;Save)->
```

The previous figure shows that the latest disk maintenance was performed on May 11th. Check the log to see what disk maintenance was performed.

STEP 2: Verify the error is real and is at the same location.

Two steps can be used to verify the error. First, perform reads on the track in question to see if any media-related errors occur. If errors occur, the sector is bad and needs slipping. If errors do not occur, then check the current list of flaws and see if any old flaws are on the same head within one cylinder of the new flaw. If this condition is true, then a media flaw which was detected on another cylinder is marginally affecting this track so the sector should still be slipped.

The following figure shows the two steps to verify the error.

Figure dev5130–58, Use of Verify and List Commands Example

```
(D1;Save)-> verify 10 times 356 1 19
verify_format: pass # 4
dev5130 drv  1 ERROR 13(cntlr) Soft ECC error
  Cyl: 356 Hd: 1 Sect: 19
7
dev5130 drv  1 ERROR 13(cntlr) Soft ECC error
  Cyl: 356 Hd: 1 Sect: 19
10
(D1;Save)-> list
Summary of all flaws on drive 1 serial number 03658:
 CYL HD SEC  BCAI   LEN TYPE  ERR SRC | CYL HD SEC  BCAI   LEN TYPE  ERR SRC
   ---------- list of all flaws for this drive prints here ----------
```

The *verify* command shows whether the error repeats when performing reads only. The *list* command shows all flaws that have been slipped. Check this list for flaws near the new flaw. If executing either of these commands indicate that the flaw should be slipped, then continue to the next step. Otherwise, use the *data_verify* and *pattern_test* commands which perform writes before reads. The error may only show up when the data is written and then read.

STEP 3: Slip the bad sector(s)

To slip cylinder 356 head 1 sector 19, enter the commands and data shown in the following figure:

Figure dev5130–59, Use of Slip Command Example

```
(D1;Save)-> slip
Type 'h' for help with slip commands
slip (D1;Save;Sector)-> 356 1 19
slip (D1;Save;Sector)-> execute

Summary of new flaws on drive 1 serial number 03658:
 CYL HD SEC  BCAI   LEN TYPE  ERR SRC | CYL HD SEC  BCAI   LEN TYPE  ERR SRC
 356  1  19 15200  4825      NONE NEW |

        Are you sure inputs are ready for slipping? [yn] (y) -> y

 Number of spares per track: 1
 cyl hd sec  bcai  len  action              additional information
---- -- --- ----- ----- ------- ------------------------------------------
 356  1  19 15200  4825 slipped

slip (D1;Save;Sector)-> quit
(D1;Save)->
```

The sector is now slipped.

If more than one flaw is to be slipped, enter all flaws before entering the *execute* command at the `slip (D1;Save)->` prompt.

STEP 4: Verify the entire disk to see if any other grown errors occur.

The *verify_format* command can be used to verify that the entire usable part of the disk is error-free. To verify the entire usable part of the disk, enter the *verify_format* command and data as shown in the following figure:

Figure dev5130–60, Use of Verify Format Command Example

```
(D1;Save)-> verify 0 0 0 to end
verify_format: pass # 1
(D1;Save)-> quit
```

Since errors did not occur when the verify was executed, the entire disk is readable. This verify may not detect intermittent errors which only a long-term read of the disk would find, but the verify does perform a quick check for flaws on the disk. If any additional flaws occur during this verify, repeat the above steps to slip the new flaws.

Manufacturer's Defect List and Grown Defect List

All drives on Interphase 4200 V/SMD controllers have the innermost cylinder reserved for five copies of the Manufacturer's Defect (MD) list and Grown Defects (GD) list. Drives on Interphase 4201 V/ESDI controllers use the next to the innermost cylinder. This is due to the fact that the original Manufacturer's Defect map is recorded on the innermost cylinder of ESDI drives and is not overwritten by this formatter. Unfortunately, SMD drives have part of the original Manufacturer's Defect map written to every track on the drive so there is no way to preserve it.

Since UNIX must not write to the defect data copies, the UNIX disk parameters file */etc/disktab* specifies one less cylinder than the disk actually has.

Defect Cylinder Organization on Drives

The defect cylinder on a drive has the following organization:

head 0 — 1st copy of defect data
head 1 — 2nd copy
head 2 — 3rd copy
head 3 — 4th copy
head 4 — 5th copy
heads 5-9 — continuations of 1st through 5th copies, respectively (if needed)
heads 10-14 — continuations of 1st through 5th copies, respectively (if needed)
heads 15-19 — continuations of 1st through 5th copies, respectively (if needed)

The MD list starts in sector 0 of the first track as defined above and continues on consecutive tracks. The GD list starts in the next sector following the last sector used by the MD list.

Format of Manufacturer's Defect List

The Manufacturer's Defect (MD) list has the following format:

```
word 0            - Magic Number - 0x492ab20e
word 1            - Version Number of formatter when Manufacturer's defect
                    list was written. The number 300 in the lower halfword
                    means version 3.00 which is the initial version of this
                    formatter.
                    The upper halfword is set to zero and is unused for now.
word 2            - Date (seconds since Jan 1, 1970)
word 3            - Number of Manufacturer's Defect Entries  (Assume m entries)
word 4-6          - First of Manufacturer's Defect Entries
     :
word 3m+4 - 3m+6 - Last of Manufacturer's Defect Entries
```

Format of Grown Defect List

The Grown Defect (GD) list starts in the next available sector after the Manufacturer's Defect (MD) list. It is therefore necessary to read the number of entries in the MD list before the GD list can be located.

The GD list has the following format:

```
word 0            - Magic Number - 0x92b41fe7
word 1
    halfword 0    - Control bits (in binary)
                    sssspppp XXXXXXXm

                    where ssss is the pattern set used during pattern test.
                    The pattern sets are defined in the description of
                    Subtest 301, Format and Pattern Test.
                    pppp is the index (1-based) into the
                    pattern set. If pppp is 1111, then no pattern testing
                    has been done on this drive. If pppp is 0000, then
                    pattern testing was completed. The bit labeled 'm'
                    is set if the MD list was ignored. This is an option
                    at format setup (Subtest 300, Format Setup).

    halfword 1    - Version Number of formatter when Grown Defect List
                    was written. Two implied decimal places. I.E.- the
                    number 300 will mean version 3.00.
word 2            - Date (seconds since Jan 1, 1970)
word 3-10         - Serial Number (up to 31 characters)
word 11           - Number of Grown Defect Entries  (Assume n entries)
word 12-14        - First of Grown Defect Entries
     :
word 3n+12 - 3n+14 - Last of Grown Defect Entries
```

Format of Entries in the Manufacturer's Defect List and Grown Defect List

Each entry in both the Manufacturer's Defect (MD) list and Grown Defect (GD) list have the following format:

Bytes	Description
0-1	Cylinder
2	Head
3	Sector position (logical based on no slipped sectors or spares)
4	Encoded Bit field
	11110000 - Unused in *dev5180*
	00001111 - Error program detected - definitions of these bits will change depending on the formatter used
	XXXX0000 - not attempted yet or none detected
	XXXX0001 - soft ECC
	XXXX0010 - header checksum
	XXXX0011 - invalid header pad
	XXXX0100 - hard ECC
	XXXX0101 - sector not found
	XXXX0110 - invalid data sync
	XXXX0111 - invalid header sync
	XXXX1000 - unrecognizable header
	XXXX1001 - mapped header error
	XXXX1010 - this code is unused
	XXXX1011 - other error
5-7	Byte Count after Index

8 Error source - Bit field
XXXXXX00 - User input
XXXXXX01 - Program-detected
XXXXXX10 - Manufacturer's Defect Map
XXXX1XXX - Can't map this flaw - map-track command failed
XXX1XXXX - Track is defective
XX1XXXXX - More than 4 flaws on this track
X1XXXXXX - New entry
1XXXXXXX - Ignore this error

9-11 Bit length

Track Relocation Area Description

The first five sectors of each of the last five tracks in the track relocation area (track map log and alternate track area) are reserved for holding one copy of the track map log.

Each entry in the log corresponds to a track in the alternate track area. The first entry in the log corresponds to the last track - 5 on the innermost cylinder of the track relocation area. The second entry corresponds to the last track - 6 and so on.

The file */mnt/bin/lib/DB_diskfmt* defines the number of cylinders that are set aside for the track map log and alternate track area. At least one cylinder must be dedicated for the track map log and alternate track area. As of version 3.00 of this formatter, the technique for calculating the number of cylinders is 0.005 * total number of cylinders rounded up. If */mnt/bin/lib/DB_diskfmt* defines more cylinders than are necessary to total 636 tracks (the maximum number of entries allowed in the track map log), then only the innermost 636 tracks of the alternate track area are set aside as alternate tracks. So, tracks beyond those defined in the */mnt/bin/lib/DB_diskfmt* file are not used.

NOTE

If any media flaws fall in the alternate track area, the track is mapped to itself.

For example, on the NEC 2363 drive, if cylinder 1021, head 20 is bad, then the 5th word of the track map log is set to cylinder 1021 head 20 so that it is not used by other tracks.

The association of entries with tracks on a 1 GByte NEC 2363 drive which has cylinders 0-1023, heads 0-26, and sectors 0-66 is the following:

Track Relocation Area	Entry	Cylinder	Head
Track map log	Log copy 1	1021	26
	Log copy 2	1021	25
	Log copy 3	1021	24
	Log copy 4	1021	23
	Log copy 5	1021	22
Alternate track area	Alt trk 0	1021	21
	Alt trk 1	1021	20
	:	:	:
	Alt trk 21	1021	0
	Alt trk 22	1020	26
	Alt trk 23	1020	25
	:	:	:
	------- etc -------		

Format of the Track Map Log

The track map log has the following format:

```
word 0          - Magic Number - 0xca29e40b
word 1          - Version Number of formatter when written. The number
                  300 in the lower halfword will mean version 3.00.
                  The upper halfword is set to zero and is unused for now.
word 2          - Date (seconds since Jan 1, 1970)
word 3          - Number of Track Map Entries (one word per entry)
word 4          - Entry 0
                  Upper halfword - cylinder of bad track
                  Lower halfword - head of bad track
words 5 - 639   - Remaining 635 entries
```

Disk Parameters File, *DB_diskfmt* Description

The disk parameters file, */mnt/bin/lib/DB_diskfmt*, contains information about disk drives. This information is required to be able to format or test new drives. Each line in the file contains a number of fields separated by one or more spaces. Comments start with a # in column 1. To add new drives, create a new entry with all the fields defined, and then add the drive to the */ioconfig* file. As of the time of this printing, the *DB_diskfmt* file contains the following information for all CONVEX machines:

Figure dev5130–61, Contents of the *DB_diskfmt* File

```
# DB_diskfmt - file of disk parameters
# >>>> WARNING - DO NOT USE 'diskfmt' TO FORMAT! It is no longer compatible
# >>>>           with the CONVEX FORMAT! Instead, format MBUS-attached drives
# >>>>           with 'dev4110' and VME-attached drives with 'dev5130'.
# KEY FOR DRIVE NAMES (unformatted capacity is given in parentheses):
#  Name          Description            Name         Description
# DKD-001       Fujitsu Eagle (452MB) DKD-008,208  NEC 2363 (1080MB)
# DKD-002       CDC 9766 (300MB)      DKD-214      Hitachi DK514-38 (356MB)
# DKD-005,206   NEC 2352 (500MB)
#------- XYLOGICS 450/451 SMD CONTROLLER (MBUS) -------
#  a    b    c   d  e  f    g     h    i j k  l  m   n    o  p
DKD-001 2  842 20 46 45 4800 28160 1 0 1  0  0  smd mfm y
DKD-002 0  823 19 32 31 5040 20160 1 0 1  0  0  smd mfm y
DKD-005 0  760 19 60 59 4832 36288 1 0 1  0  0  smd 2-7 y
DKD-008 1 1024 27 68 67 4816 40960 1 0 1  0  0  smd 2-7 y
#------- INTERPHASE 4201 ESDI CONTROLLER (VME) --------
#  a    b    c   d  e  f    g     h    i j k  l  m   n    o  p
DKD-214 0  903 14 51 50 4736 30240 5 5 1  8  8 esdi 2-7 n
#------- INTERPHASE 4200 SMD CONTROLLER (VME) ---------
#  a    b    c   d  e  f    g     h    i j k  l  m   n    o  p
DKD-206 0  760 19 60 59 4832 36288 5 4 1 12 12  smd 2-7 n
DKD-208 0 1024 27 68 67 4816 40960 5 6 1 16 12  smd 2-7 n
# LEGEND:
# a - drive name                Must be DKD-0XX for Multibus and DKD-2XX for
#                               VMEbus
# b - disk type                 For Xylogics controller
# c - # of cylinders
# d - # of heads
# e - # of physical sectors     Number of actual sectors excluding runt
# f - # of logical sectors      Number of physical sectors (e) minus number of
#                               spares
# g - bits per sector           Number of bits between sector pulses
# h - bytes per track           Total number of unformatted bytes per track
# i - skew                      Sector offset from one head to the next
#                               Must be 1 when using Xylogics 450/451 cntlr
# j - # of relocation tracks    .5% of number of cylinders (c). Raise
#                               fractional part to next higher whole number.
#                               Ignored by dev4110 (Multibus formatter)
# k - interleave                sector separation between consecutive sectors
#                               Currently must be 1 for Xylogics 450/451 cntlr
# l - gap 1 size                Number of halfwords in gap before header
#                               (2 bytes per halfword)
#                               Ignored by dev4110 (Multibus formatter)
# m - gap 2 size                Number of halfwords in gap following header
#                               (2 bytes per halfword)
#                               Ignored by dev4110 (Multibus formatter)
# n - drive interface           Used to determine how to read manufacturer's
#                               defect map.  Currently, smd or esdi
#                               Ignored by dev4110 (Multibus formatter)
# o - data encoding scheme      Way data is encoded on the media. Used to
#                               select patterns for pattern test.
#                               Currently mfm, 2-7 or 1-7
# p - Are spares interleaved    For Xylogics, 'y'. For Interphase, 'n'.
```

Diagnostic Cylinder Description

The diagnostic cylinder is located on the first full cylinder preceding the sector forwarding area. Cylinder 840 is the diagnostic cylinder on a Fujitsu Eagle drive, and cylinder 820 is the diagnostic cylinder on a CDC SMD drive.

Each track of the cylinder is independent of the other tracks since there is a "table of contents" stored at sector 0 of each track This table describes what is stored on the remainder of that track. The format of this table is shown below:

Figure dev5130–62, Diagnostic Cylinder Table of Contents Format

```
/* ------------------------------------------------------------------ *
 *              Diagnostic Cylinder Definitions                       *
 * ------------------------------------------------------------------ */
#define NOT_USED        0x00000000      /* position in tbl not used     */
#define NO_HDR          0x00000001      /* this sectors header deleted  */
#define TBL_CONT        0x00000002      /* sector contains tbl of cntnts*/
#define ECC_ERR         0x00000003      /* sector written with bad ecc  */
#define PATTERN         0x00000004      /* sector written with pattern  */

 struct   tbl_cont {
    int   magic_nbr;          /* identifies this as a table of contents */
    int   version;            /* version number of this table */
    int   cyltksc;            /* sector header for this sector*/
    struct {
     int   sec_cont;         /* defines contents of corresponding sector */
     int   pattern;          /* pattern or mask used to verify contents  */
    } sec_tbl[62];
    int   checksum;           /* arithmetic tally of all the above fields */
 };
```

Each track on the cylinder is formatted in such a way that sector 0 is always on the track; sector 0 is written and verified without error when the drive is formatted.

The first field in the table contains the magic number 0x84101500. If this number is not present in the first position of a table, then someone has altered the diagnostic cylinder.

The second field in the table contains the version number. This number is an ordinal number starting with one and increasing as needed. Its purpose is to allow some measure of compatibility of newer diagnostic cylinders with older software. This number is checked if an unknown entry in the sector table (sec_tbl) is encountered. If the version number in the table is greater than the version number of the software, the diagnostic cylinder is assumed to have been formatted with a newer revision of software, and the opcode in the sector table is new to the older software. Therefore, the software is not familiar with the opcode, and the entry in the sec_tbl is ignored.

The next field in the table contains a copy of the sector header (cyltksc) for the table of contents.

The next field in the table contains the sector table (sec_tbl). This table describes what is stored on the rest of the sectors in this track. The sector table consists of 62 entries of 2 int's. Each entry (0 - 61) in this table, corresponds to a sector (0 - 61) on the track. The first position in

each entry is the sector contents (sec_cont) field. If the track has more than 62 sectors, the extra sectors are not used or checked by current software. The following table describes what is currently defined:

Table dev5130–17, Defined Values for Sector Contents Field

FIELD	DESCRIPTION
NOT_USED	This sector has not been initialized and should not be checked.
NO_HDR	When this sector is read, the controller should return a 0x05 sector not found error.
TBL_CONT	This sector contains a copy of the table of contents.
ECC_ERROR	This sector contains a copy of the table of contents that has been corrupted to give some form of ECC error. The pattern field contains a mask which may be xor'ed with the magic number field to correct the error. If the mask contains 11 or fewer one bits, the controller should report a soft ECC error when this sector is read. If the mask contains more than 11 one bits, the error reported should be a hard ECC error.
PATTERN	This sector has been filled with the data contained in the pattern field. No errors should be encountered when the sector is read.

The last field in the table of contents is a checksum. This is an arithmetic tally of all the bytes in the table of contents. This value is checked before any of the data in the table of contents is used.

Error Messages

The following are error messages for the *dev5130* test. The following error format is generated from a test and is not associated with a controller or drive:

```
dev5130 ERROR 56(test)-Unable to get SPU memory
```

The following error format is generated from a test and is associated with a controller but not with a specific drive:

```
dev5130 ccu/vb/csr 7/0/e00: ERROR 94(test) No cntlr interrupt in 5 seconds
```

The last error format shown below is generated from a controller and is associated with a specific drive:

```
dev5130 drv 1 ERROR 13(cntlr) Soft ECC error
 Cyl: 356 Hd: 1 Sect: 19
```

The following are possible errors:

- 0x10(cntlr) Disk not ready (or, if a DKD-214, "Write Protected")

- 0x12(cntlr) Seek error
- 0x13(cntlr) Soft ECC error
- 0x14(cntlr) Invalid Command Code
- 0x15(cntlr) Illegal fetch and execute
- 0x16(cntlr) Invalid sector in command
- 0x17(cntlr) Illegal memory type
- 0x18(cntlr) Bus timeout
- 0x19(cntlr) Header checksum error
- 0x1a(cntlr) Disk write protected
- 0x1b(cntlr) Unit not selected (or, "Powered Off")
- 0x1c(cntlr) Seek error timeout
- 0x1d(cntlr) Fault timeout
- 0x1e(cntlr) Drive faulted
- 0x1f(cntlr) Ready timeout
- 0x20(cntlr) End of medium
- 0x21(cntlr) Translation fault
- 0x22(cntlr) Invalid header pad
- 0x23(cntlr) Hard ECC error
- 0x24(cntlr) Translation error, cyl
- 0x25(cntlr) Translation error, head
- 0x26(cntlr) Translation error, sect
- 0x27(cntlr) Data overrun
- 0x28(cntlr) No index pulse on format
- 0x29(cntlr) Sector not found
- 0x2a(cntlr) ID field error-wrong head
- 0x2b(cntlr) Invalid sync in data field
- 0x2c(cntlr) No valid header found
- 0x2d(cntlr) Seek timeout error
- 0x2e(cntlr) Busy timeout
- 0x2f(cntlr) Not on cylinder
- 0x30(cntlr) RTZ timeout
- 0x31(cntlr) Invalid sync in header
- 0x3f(cntlr) No heads specified
- 0x40(cntlr) Unit not initialized
- 0x41(cntlr) Not used
- 0x42(cntlr) Gap specification error
- 0x42(test) No consecutive sectors found
- 0x43(test) Flaw log is full
- 0x47(test) Bad parm to calc_cyl

- 0x48(test) Bad parm to calc_hd
- 0x49(test) Bad parm to calc_sec
- 0x4a(test) IOP print utility memory error
- 0x4b(cntlr) Seek error
- 0x4b(test) Device FAILED
- 0x4c(test) Input parms don't allow write
- 0x4e(test) Diag. trk has all bad headers
- 0x4f(test) Diag. cylinder bad
- 0x50(cntlr) Sectors/track error
- 0x50(test) Bad data compare on diag. cyl
- 0x51(cntlr) Bytes/sector spec error
- 0x51(test) No err. Hdr-not-found expected
- 0x52(cntlr) Interleave spec factor
- 0x52(test) Soft ECC error did not occur
- 0x53(cntlr) Invalid head address
- 0x53(test) Hard ECC error did not occur
- 0x54(cntlr) Invalid cylinder addr
- 0x54(test) Data compare err on diag cyl
- 0x55(test) Setup failed - aborting test
- 0x56(test) Unable to get SPU memory
- 0x57(test) Track map log is full
- 0x58(test) No defect lists could be read
- 0x59(test) Can't read Manufacturer's defects
- 0x5a(test) New flaws exceeded user limit
- 0x5b(test) No copies successfully written
- 0x5c(test) Less than 3 good copies of defect lists
- 0x5d(cntlr) Invalid DMA xfer count
- 0x5f(test) Hardware is suspected to be bad
- 0x60(cntlr) IOPB failed
- 0x60(test) Drive is previously formatted
- 0x61(cntlr) DMA failed
- 0x61(test) Drive is not previously formatted
- 0x62(cntlr) Illegal VME address
- 0x62(test) Unable to read track headers
- 0x63(test) Unable to access main memory
- 0x64(test) Mapped track has invalid headers
- 0x65(test) Alternate track has invalid headers
- 0x66(test) Incorrect alloc of pattern space
- 0x67(test) Message received was not handshake

- 0x68(test) Incorrect handshake message format
- 0x69(test) Defect list to long to fit on disk
- 0x6a(cntlr) Unrecognized header field
- 0x6a(test) Prev. formatted drive appears unformatted
- 0x6b(cntlr) Mapped header error
- 0x6b(test) User terminated drive
- 0x6c(test) Controller firmware is out of date
- 0x6d(test) Bad data written by Format with data
- 0x6f(cntlr) No spare sector enabled
- 0x77(cntlr) Command aborted
- 0x78(cntlr) ACFAIL detected
- 0x80(test) Data compare error
- 0x81(test) Seek requested with a seek count = 0
- 0x85(test) Desired IOPB not in active chain
- 0x86(test) Message received on wrong subqueue
- 0x87(test) Wrong subqueue active and locked
- 0x88(test) Wrong subqueue active and MBS error
- 0x89(test) Wrong subqueue active, error invalid
- 0x8a(test) river executed for no reason
- 0x8c(test) ntlr busy after hard error
- 0x92(test) EGOS routine wndw_alloc returned 0
- 0x93(test) Task init attempt-error pending
- 0x94(test) No cntlr interrupt in 5 seconds
- 0x96(test) Write/Read error in controller regs
- 0x9a(test) Finished task but int. state wrong
- 0x9b(test) Controller is not present
- 0x9c(test) Sector interleave or skew error
- 0x9d(test) Bad cylinder address after seek
- 0xa0(test) Expected error did not occur
- 0xa2(test) No free IOPBs for retry
- 0xa3(test) Controller didn't finish IOPB
- 0xa4(test) Unknown error reported by cntlr
- 0xa5(test) Internal Defect log is full
- 0xa6(test) Controller doesn't respond
- 0xa7(test) Track doesn't contain flaw data
- 0xa8(test) Cntlr reporting board not ok
- 0xa9(test) Software error-Invalid verify
- 0xaa(test) Cntlr GO/BUSY set after diag cmd
- 0xab(test) Header contains bad cyl number

- 0xac(test) Header contains bad head number
- 0xad(test) Attempt to configure cntlr failed
- 0xae(test) Unexpected value in cntlr CSR
- 0xaf(test) Bad cyl, hd, or sec in IOPB
- 0xb0(test) NI with more than 1 spare
- 0xc0(cntlr) Both bits set (from appl. note)
- 0xc1(cntlr) MSE without init long (from appl. note)
- 0xff(cntlr) Command not implemented

Special Error Messages for *dev5130*

In some circumstances, a certain set of error messages are displayed if the peripheral is not powered on, is write protected, or is cabled incorrectly. The test gives the user several options to proceed with, depending on the circumstances. The following examples illustrate these type of error messages and user options that are presented. The first example illustrates the messages produced when the peripheral is not ready (ie., power is not on or a cable is not connected). The second example illustrates the messages produced when the peripheral is write protected and an operation attempts a write.

> **NOTE**
>
> In the following examples, all **boldface** entries are user entered information.

Figure dev5130–63, Drive Not Ready Error Example

```
(D1;Save)-> alternate 0 to 1000
Beginning alternate seeks (1 times)...
dev5130 drv 1 1b(cntlr) Unit not selected
  Cyl:   0 Hd: 0 # Seeks:2
  IOPB: opt  err  cyl hd/s  cnt bufh buf1 bmem inr  dma ptrh ptr1 imem skew
       8102 821b 0000 0000 0001 0001 2000 033d 0100 1000 0000 0000 0000 0000
Attempt to fix the problem. You can issue UNIX commands if it helps.
Then enter on of the following:
        <CR> to retry the operation
        'nofix' if unable to fix the problem
UNIX command, <CR> for retry, or nofix: RETURN

dev5130 drv 1 1b(cntlr) Unit not selected
  Cyl:   0 Hd: 0 Sect:  0 # Seeks:2
  IOPB: opt  err  cyl hd/s  cnt bufh buf1 bmem intr  dma ptrh ptr1 imem skew
       8102 821b 0000 0000 0001 0001 2000 033d 0100 1000 0000 0000 0000 0000
Attempt to fix the problem. You can issue UNIX commands if ti helps.
Then enter on of the following:
        <CR> to retry the operation
        'nofix' if unable to fix the problem
UNIX command, <CR> for retry, or nofix: noflx

(D1;Save)-> alternate 20 times 0 to 1000
Beginning alternate seeks (20 times)....
dev5130 drv 1 1b(cntlr) Unit not selected
  Cyl:   0 Hd: 0 # Seeks:21
  IOPB: opt  err cyl  hd/s  cnt bufh buf1 bmem inr   dma ptrh ptr1 imem skew
       8a02 821b 0000 0000 0001 0000 0000 033d 0100 1000 0000 0000 0000 0000
```

Figure dev5130–64, Write Protect Error Example

```
(d1;Save)-> pattern_test 1022 10 30 with 0
     Patterns used:
      00000000
        No data has been previously saved. Savin this track
        Data save operation complete
 pass #1
dev5130 drv 1 1a(cntlr) Disk write protected
  Cyl:1022 Hd:10 Sect: 30 # Seeks:2
  IOPB: opt  err  cyl hd/s  cnt bufh buf1 bmem intr  dma ptrh ptr1 imem skew
       8202 821a 03fe 0a1e 0001 0005 2000 033d 0100 1000 0000 0000 0000 0000
Attempt to fix the problem. You can issue UNIX commands if it helps.
Then enter one of the following:
        <CR> to retry the operation
        'nofix' if unable to fix the problem
UNIX command, <CR> for retry, or nofix: nofix
        Restoring data to track

dev5130 drv 1 1a(cntlr) Disk writ protected
  Cyl:1022 Hd:10 Sect: 0 # Seeks:2
  IOPB: opt  err  cyl hd/s  cnt bufh buf1 bmem intr  dma ptrh ptr1 imem skew
       8202 821a 03fe 0a00 0001 0005 2000 033d 0100 1000 0000 0000 0000 0000
                        1 attempts to write sector failed
                        what to do [# of retries/force/skip] (1) ->skip
```

Figure dev5130–65, Power Off Error Message

```
(D1;Save)-> verify_format 0 0 0
verify_format: pass #1
dev5130 drv 1 10(cntlr) Disk no ready
  Cyl:   0 Hd: 0 Sect:  0 # Seeks:2
IOPB: opt  err  cyl hd/s  cnt bufh buf1 bmem inr  dma ptrh ptr1 imem skew
    8102 8210 0000 0000 0001 0001 2000 033d 0100 1000 0000 0000 0000 0000
Attempt to fix the problem. You can issue UNIX commands if it helps.
Then enter on of the following:
        <CR> to retry the operation
        'nofix' if unable to fix the problem
UNIX command, <CR> for retry, or nofix: nofix
```

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dev5210

VMEbus STC Tape Unit Controller Test

Overview

The *dev5210* test is a functional test for the CONVEX VMEbus Tape Controller (VBTC) and its connected tape unit(s). The VBTC provides a connection to a magnetic tape drive unit that is based on the STC interface. In general, this test attempts to force most software forcible formatter and controller errors and verify that either the formatter or controller can detect them.

This functional test is modeled to test the STC 2921, STC 2922, and STC 1968 drives. In addition, the test supports testing of the Fujitsu 243XL. Read/Write type testing is conducted at recording densities of:

- **800 bpi**—Nonreturn to Zero (NRZI)
- **1,600 bpi**—Phase Encoded (PE)
- **6,250 bpi**—Group Coded Recording (GCR)

Specifically, *dev5210* is designed to accomplish the following:

- Verifies the functional ability of the VBTC to operate in the CONVEX VMEbus I/O environment. This includes main memory access and interrupt generation. In addition, the FIFO is pattern tested along with verification of its ability to detect parity errors.
- Verifies 14 of the 15 supported STC interface commands. The controller's ability to use data chaining on transfers and pipeline commands is tested under normal and error conditions.
- Verifies the ability of the VBTC to detect most software forcible formatter and controller errors. It insures that the VBTC can recover from bus errors.
- Verifies that the cable interface between the controller and the drive is operational.
- Provides an interactive debugger that can execute commands from a script file. This allows more debug flexibility.

Channel Control Unit (CCU) communications utilize the Event Governed Operating System (EGOS) and the Message Based System (MBS) used by CONVEX UNIX. The intent is to test the communication paths that are used in a normal operating environment.

Most subtests implement an error recovery scheme to minimize the impact of media errors. Although media errors are minimized at most points the user may select a pattern that will stress data recovery. As a result, the test requires that tape media be in adequate condition. In most write subtests, identification data is written in each block. This is used to verify positional coordinates on the tape.

The following table lists all of the STC tape commands and depicts which ones are tested:

Table dev5210–1, STC Interface Commands Tested

COMMAND DESCRIPTIONS					
Number	**Mnemonic**	**STC code**	**Function**	**Type**	**Tested**
1	*NOP*	0x00	No Operation	Diagnostic	Yes
2	*LWR*	0x07	Write to Read Loopback	Diagnostic	Yes
3	*DMS*	0x02	Diagnostic Mode Set	Diag/Norm	Yes
4	*CLR*	0x01	Drive Clear	Normal	Yes
5	*REW*	0x0e	Rewind to BOT	Normal	Yes
6	*RUN*	0x0f	Rewind to BOT and Unload	Normal	No
7	*ERG*	0x0d	Erase Gap	Normal	Yes
8	*WRT*	0x06	Write Block	Normal	Yes
9	*RDF*	0x04	Read Forward Block	Normal	Yes
10	*RDB*	0x05	Read Backward Block	Normal	Yes
11	*FSB*	0x0b	Forward Space Block	Normal	Yes
12	*BSB*	0x09	Backward Space Block	Normal	Yes
13	*WTM*	0x0c	Write Tape/File Mark	Normal	Yes
14	*FSF*	0x0a	Forward Space File	Normal	Yes
15	*BSF*	0x08	Backward Space File	Normal	Yes

Related Documents

This test description is intended as a reference for users who have a good understanding of the VBTC and VIOP, and for those who have a basic understanding of tape drives and magnetic tape recording principles. Specifically, this test description assumes familiarity with Storage Technology Corporation's *StorageTek Standard Interface* (STC interface). The following table lists several documents that may provide additional information that is not contained within this test description:

Table dev5210–2, Related Documents

Document Title	Document Origin
STC Compatible Multibus Controller Specification	CONVEX
VME Tape Controller Difference Document	CONVEX
VME IOP Difference Document	CONVEX
The STC 2920 Maintenance Manual	STC
The STC 1960 Maintenance Manual	STC
The Fujitsu 2xXL Maintenance Manual	Fujitsu

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test:

Table dev5210–3, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
VIOP	VIOP
VBCU	PIA
VBTC[2]	VBCU
Tape Drive	VBTC[2]
	Tape Drive

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

[2] VBTC represents VMEbus Tape Controller

Test Invocation

The *dev5210* test executes under the Diagnostic Shell (Dshell) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order. To invoke the *dev5210* test, use the procedure shown in "Figure dev5210–1, Initial Test Invocation Sequence." All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

NOTE

Use the following test invocation sequence for the initial invocation of *dev5210* or when the state of the machine is unknown. Also, the following invocation sequence should be used if any hard errors have occurred since the last system initialization.

Figure dev5210–1, Initial Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev5210 [-c [class number(s)]] [-s [subtest number(s)]] [-dnqV] [-f FILE] [+>filename] RETURN
```

> **NOTE**
>
> After entering **dshell**, specific Dshell parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev5210** executes all *dev5210* subtests sequentially. Execute a specific class(es) of subtest(s) or one or more individual subtests by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual.

The following list defines the remaining dash options:

- -d Enter Debugger (no subtests are executed)
- -n Do not actually execute any subtest (used to create a parameter file without actually executing any subtest)
- -q Quick startup (use previous parameters from last test invocation—same as entering **dev5210x**, refer to the "Alternate Test Invocation Sequence")
- -V Print version string (compilation date of test–last modification date).
- -f *FILE* Use *FILE* as the parameter save file. If this option is omitted, */tmp/dev5210.tmp* is used as the parameter file.

The [+>*filename*] option allows the test results to be appended to *filename*.

> **NOTE**
>
> The following alternate test invocation procedure is optimal when invoking *dev5210* multiple times. Using this invocation sequence insures that the test is invoked and executed with all of the setup parameters supplied when the test was last executed with the initial invocation sequence.

Figure dev5210–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
:test dev5210x [-c [class number(s)]] [-s [subtest number(s)]] [-dnqV] [-f FILE] [+>filename] RETURN
```

The only difference in this alternate invocation sequence is the **x** after **dev5210**. When invoking *dev5210* in this manner, no prompts are displayed. The diagnostic obtains all prompt information from the parameter file created when the initial invocation sequence was performed.

Also note that **mminit -s** is only required if the state of the machine is unknown or if hard errors have occurred since the last system initialization.

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The "Test Parameter Menu" in Figure dev5210–3, shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses in the figure appear sequentially on the screen, one line at a time. The figure illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. The numbers displayed on the screen during testing may not correspond to those shown in the example, as the questions illustrated are examples only.

For help or information during test parameter entry, enter one of the following characters followed by a (RETURN):

Table dev5210–4, Getting Help During Test Parameter Entry

Character	Description
:?	Reviews previous entries
?	Provides specific help where available

After the desired help information displays, the system redisplays the last prompt.

Figure dev5210–3, Test Parameter Menu

```
                    ENTER TEST PARAMETERS

        []      Encloses allowed input ranges or values
        ()      Encloses the default value
        ^       Returns to the previous prompt
        :nn     Returns to the prompt # nn
        :       Returns to the first unsatisfied prompt
        :?      Reviews previous entries
        ?       Provides specific help where available

 1: Select Configuration File [<filepath>,?]      (/ioconfig) -> RETURN

                  PERIPHERAL CONFIGURATION DATA
            CCU    Chassis   Type    CSR   Int Unit   Type
        -------- ------- -------- ------ --- ---- --------
         1) viop  3     0    MTC-201  0x0600  1   1   MTD-204
         2) viop  3     0    MTC-201  0x3fc0  4   0   MTD-201

        *** Enter 0 for manual configuration ***

 2: Select Configuration File Entry to Test [0,1-2,?]     (1) -> 0
 3: Display VBTC Configuration Help [y,n,?]               (y) -> n
 4: VME IOP Number [3-7,?]                                (3) -> 3
 5: VME Chassis Number [0-1,?]                            (0) -> 0
 6: VMEbus Base Address of the Controller [0x0-0xffff,?]
                                                  (0x600) -> 0x600
 7: VMEbus Interrupt Level of the Controller [1-7,?]      (1) -> 1
 8: Tape Unit Number [0-7,?]                              (1) -> 1

           ** Tape Drive models **
    1:     Storage Technology Corp. 2921 ..... MTD-201
    2:     Storage Technology Corp. 2922 ..... MTD-204
    3:     Storage Technology Corp. 1963/1968 ..... MTD-202
    4:     Fujitsu 2436-L1 ..... MTD-203

 9: Tape Drive Type [1-4,?]                               (2) -> 2
10: Use Standard Defaults for Other Options [y,n,?]       (y) -> n

           ** Tape Spool Size in Feet **
    1:      600 ft.
    2:     1200 ft.
    3:     2400 ft.
    4:     3600 ft.

11: Select Mounted Tape Spool Size [1-4,?]                (1) -> 1
12: Run EOT Sensor Subtest #701 [y,n,?]                   (y) -> y
```

Figure dev5210–3, Test Parameter Menu (continued)

```
            ** Available Data Transfer VMEbus Address Modifiers **
    1:      Standard Supervisory Access (16 bit) (0x3d)
    2:      Standard Non-Supervisory Access (16 bit) (0x39)

13: Data Transfer VMEbus Address Modifier [1-2,?]          (1) -> 1

            ** Available Tape Velocities (IPS) **
    1:       50
    2:      100

14: Standard Tape Velocity [1-2,?]                         (2) -> 2
15: Standard Tape Block Size [16-16777216,?]            (8192) -> 8192
16: Large Tape Block Size [262144-16777216,?]       (16777216) -> 16777216
*** WARNING:
    Due to insufficient tape length, the selected Large Block of 16777216
    will be reduced to 11520000 when using PE   recording format.

  ** Printer On/Off Enable/Disable Options (bit mapped) **
    0x0001: Enable printer ON string before error
    0x0002: Enable printer OFF string after error

17: Select Printer On/Off Mode [0x0-0x3,?]                 (0x0) -> 0x3
18: Printer On Character Sequence (before error)
    [<printer on string>,?]                          (\033[?5i) -> \033[?5i
19: Printer Off Character Sequence (after error)
    [<printer off string>,?]                         (\033[?4i) -> \033[?4i
20: Use Standard Debug Setup [y,n,?]                       (y) -> n
21: Pattern for Write/Read Subtests [<hexadecimal pattern>,?]
                                                     (0x6db6) -> 0x6db6
22: Maximum Media Error Retry Count [0-999,?]              (9) -> 9
23: Retry Formatter Correctable Media Errors [y,n,?]       (n) -> n

            ** Tape Media Error Logging Methods (bit mapped) **
    0x0001: After Test Completion
    0x0002: After Each Subtest
    0x0004: Upon Occurrence (Real time)

24: Select Media Error Logging Method [0x0-0x7,?]          (0x1) -> 0x7

            ** Available Data Miscompare Dump Modes **
    1:      Separate Expected and Actual Values into Two Blocks.
    2:      Mix Expected and Actual Values (xx/xx).
    3:      Only Show Bytes that Miscompare.

25: Select Data Miscompare Display Mode [1-3,?]            (2) -> 2
26: Enter Data Miscompare Line Dump Count [1-1000,?]       (4) -> 4
```

Figure dev5210–3, Test Parameter Menu (continued)

```
            ** VBTC register dump modes **
     1:     After Error
     2:     After Each Command Completion
     3:     Never

27: Select Controller Register Dump Mode [1-3,?]          (3) -> 3

  ** USER Debug Options (bit mapped) **
    0x0001: Disable Asynchronous Command Mode
    0x0002: Disable Multi-Record Buffering
    0x0004: Disable Reset of Controller After ^C
    0x0008: Disable Hard Error Trapping (logging)
    0x0010: Enter Debugger After an Error Occurs
    0x0100: Pause AFTER each CCU driver command is returned
    0x0200: Show each CCU driver message AFTER it is returned
    0x0400: Pause BEFORE each CCU driver message is sent
    0x0800: Show each CCU driver message BEFORE it is sent

28: User Debug Option Mask [0x0-0xfff,?]                (0x0) -> 0xfff
29: Enter OK, or :NN to return to question NN [OK]       (OK) -> OK
```

NOTE

In the previous figure, a warning statement (see prompt #16) is printed because the selected tape length for the displayed density is not large enough to hold the large tape block selected. The test automatically compensates for this by changing the large tape block size to match the tape length. In all cases, the maximum large tape block size is limited by the amount of contiguous physical memory present in the target system and the maximum tape length. It is important to note that *dev5210* only compensates for insufficient tape length in the data chain mode read/write tests.

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

When all prompts are answered, the screen displays a TEST PARAMETER SUMMARY which displays the prompts that were answered and their responses. The following figure illustrates an example of a TEST PARAMETER SUMMARY screen. The actual values and responses vary according to the input.

Figure dev5210–4, Sample Test Parameter Summary

```
                    TEST PARAMETER SUMMARY

Select Configuration File                                  : /ioconfig
Select Configuration File Entry to Test                    : 0
Display VBTC Configuration Help                            : y
VME IOP Number                                             : 3
VME Chassis Number                                         : 0
VMEbus Base Address of the Controller                      : 0x600
VMEbus Interrupt Level of the Controller                   : 1
Tape Unit Number                                           : 1
Tape Drive Type                                            : 2
          -> Storage Technology Corp. 2922 <-
Use Standard Defaults for Other Options                    : n
Select Mounted Tape Spool Size                             : 1
          ->  600 ft. <-
Run EOT Sensor Subtest #701                                : y
Data Transfer VMEbus Address Modifier                      : 1
          -> Standard Supervisory Access (16 bit) (0x3d) <-
Standard Tape Velocity                                     : 2 (100 IPS)
Standard Tape Block Size                                   : 8192
Large Tape Block Size                                      : 16777216
Select Printer On/Off Mode                                 : 0x0003
          -> Enable printer ON string before error <-
          -> Enable printer OFF string after error <-
Printer On Character Sequence (before error)               : \033[?5i
Printer Off Character Sequence (after error)               : \033[?4i
Use Standard Debug Setup                                   : n
Pattern for Write/Read Subtests                            : 0x6db6
Maximum Media Error Retry Count                            : 9
Retry Formatter Correctable Media Errors                   : n
Select Media Error Logging Method                          : 0x0007
          -> After Test Completion <-
          -> After Each Subtest <-
          -> Upon Occurrence (Real time) <-
Select Data Miscompare Display Mode                        : 2
          -> Mix Expected and Actual Values (xx/xx). <-
Enter Data Miscompare Line Dump Count                      : 4
Select Controller Register Dump Mode                       : 3
          -> Never <-
User Debug Option Mask                                     : 0xfff
          -> Disable Asynchronous Command Mode <-
          -> Disable Multi-Record Buffering <-
          -> Disable Reset of Controller After ^C <-
          -> Disable Hard Error Trapping (logging) <-
          -> Enter Debugger After an Error Occurs <-
          -> Pause AFTER each CCU driver command is returned <-
          -> Show each CCU driver message AFTER it is returned <-
          -> Pause BEFORE each CCU driver message is sent <-
          -> Show each CCU driver message BEFORE it is sent <-
Enter OK, or :NN to return to question NN                  : OK
```

Initialization Sequence for *dev5210*

After the last prompt is entered, and before subtest code execution, the following events occur:

- The diagnostic determines if the test was invoked for quick startup (i.e., dev5210x or dev5210 -q). If so, the diagnostic reads the test parameters from the specified parameter file (default parameter file is */tmp/dev5210.tmp*). If not, the input to the parameters are written to the parameter file (default or user specified).
- The largest contiguous main memory space after the first 2 Mbytes is located and reserved for use by *dev5210*.
- The diagnostic checks to see if the CCU is already loaded with the *dev5210* CCU driver. If the driver is not loaded, the CCU is reloaded. After the load completes, the driver is configured for EGOS and then the EGOS probe message starts the driver.
- The CCU driver is passed the current test parameters (i.e., retry information).

> **NOTE**
>
> The file */mnt/boot_db* is used to determine what memory is installed. If this file is nonexistent, it can be created by entering: **scn_util -b > /mnt/boot_db** from the **(spu)>** prompt.

After all the above events have occurred, the test code is started.

Prompt Explanations

The test parameter prompts are repeated and explained in the following paragraphs.

```
1: Select Configuration File [<filepath>,?]        (/ioconfig) ->
```

This option allows specification of an alternate */ioconfig* file. The file must still be in the same format as a conventional */ioconfig* file.

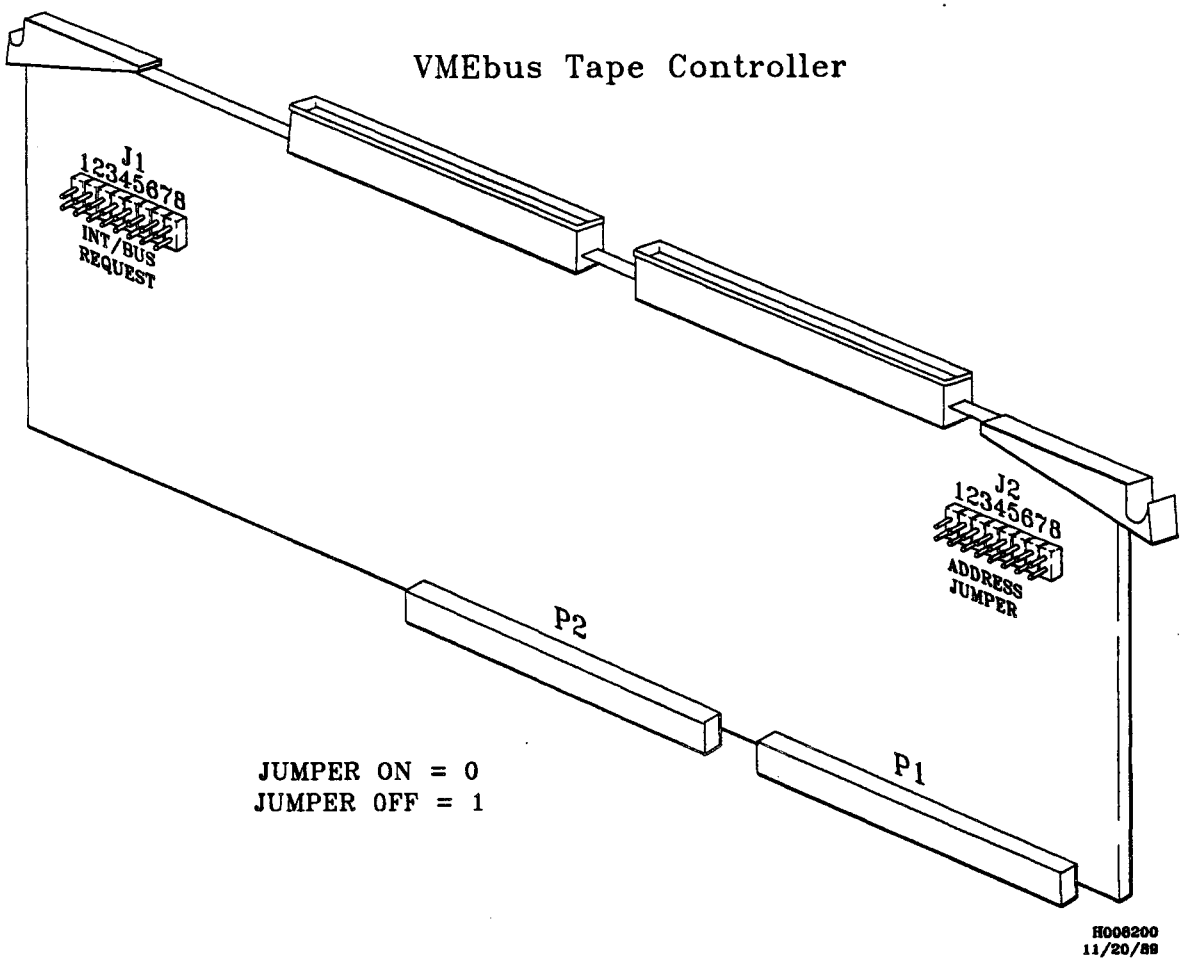
```
                PERIPHERAL CONFIGURATION DATA
    CCU     Chassis   Type     CSR    Int Unit   Type
 -------- ------- -------- ------ --- ---- --------
1) viop  3     0    MTC-201  0x0600  1   1   MTD-204
2) viop  3     0    MTC-201  0x3fc0  4   0   MTD-201
     *** Enter 0 for manual configuration ***
2: Select Configuration File Entry to Test [0,1-2,?]      (1) ->
```

Above, the applicable */ioconfig* file entries (if any) are listed. To select a predefined controller configuration entry from the */ioconfig* file, enter the number that is found to the left of the desired entry. Entering a **0** allows each item within the controller configuration entry to be independently specified. If most (but not all) of the items associated with a given entry in */ioconfig* file are desired, select the number for that entry, backup to this prompt via the caret command (SHIFT) **6**), and then specify **0** the second time. This causes the default values for the independent items to be the same as the originally selected entry.

```
3: Display VBTC Configuration Help [y,n,?]                    (y) ->
```

This option displays the VME tape controller information. This information is useful when installing the jumpers that determine the controller's base address and interrupt level. The VBTC has two jumper blocks which are used to set the board's base address, interrupt level, and VMEbus request level. All logic is inverted, i.e., a removed jumper sets that bit. The jumper blocks are shown in the following figure:

Figure dev5210–5, VMEbus Tape Controller Jumper Blocks



The jumper blocks are defined in the following tables:

> **NOTE**
>
> From left to right, the jumper block pin numbers on the VBTC are numbered 1 through 8. To make it easier to construct binary patterns, they are listed from 8 through 1 in the following tables. Also, the information listed in the following three tables is displayed on screen by entering **y** or **?** as response to the prompt.

Table dev5210–5, VBTC Jumper Block Pin Settings

Jumper Block 1—J1 (Upper left side of board)								
Jumper	8	7	6	5	4	3	2	1
Bit	INT2	INT1	INT0	XX	XX	XX	BR1	BR0

Table dev5210–6, VBTC Jumper Block Pin Settings

Jumper Block 2—J2 (Upper right side of board)								
Jumper	8	7	6	5	4	3	2	1
Address	A13	A12	A11	A10	A9	A8	A7	A6

Table dev5210–7, Standard Address and Interrupt Levels

VBTC #	Address	Interrupt Level	Bus Request
1	0x1000	7	3
2	0x1040	site dependent	3
3	0x1080	site dependent	3
4	0x10c0	site dependent	3

```
4: VME IOP Number [3-7,?]                                    (3) ->
```

Enter the CCU slot number for the VMEbus IOP that contains the VMEbus subsystem connected to the tape controller/drive. The CONVEX VMEbus tape controller part number is 410-001152-600.

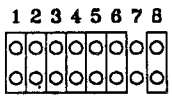
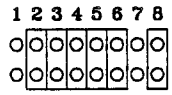
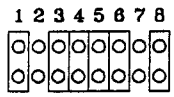
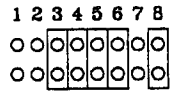
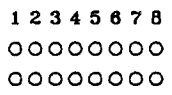
```
5: VME Chassis Number [0-1,?]                                (0) ->
```

Enter the VMEbus chassis number for the chassis where the tape controller is installed. If there is only one chassis, the number is (in most cases) 0. The CONVEX VMEbus tape controller part number is 410-001152-600.

```
6: VMEbus Base Address of the Controller [0x0-0xffff,?]
                                                    (0x600) ->
```

Enter the low-order four hexadecimal digits of the VMEbus tape controller board's base address within the VMEbus standard address space. This address is controlled by jumper block 2 (**J2**) on the controller. The typical address is 0x1000. When all the straps are removed, the controller defaults to address 0x3fc0.

Table dev5210–8, VMEbus Address Level Jumper Settings (J2)

Address	Jumper Block 2 Settings
0x1000	
0x1040	
0x1080	
0x10c0	
0x3fc0	

```
7: VMEbus Interrupt Level of the Controller [1-7,?]       (1) ->
```

Enter the CONVEX VMEbus interrupt number assigned to the VMEbus tape controller board under test. This value is between 1 and 7, inclusive. The interrupt level is selected by jumper block 1 (**J1**) on the controller. The typical level is 7. When all the straps are removed, the controller defaults to level 7.

Table dev5210–9, VMEbus Interrupt and Bus Request Jumper Settings (J1)

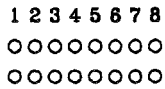
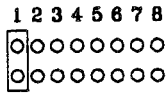
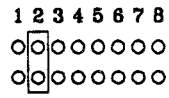
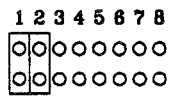
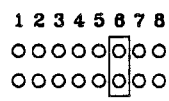
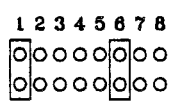
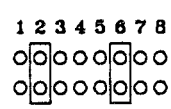
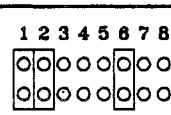
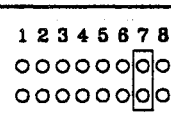
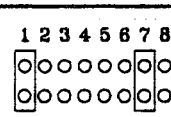
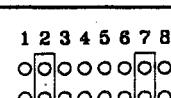
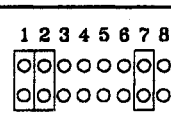
Interrupt Level	Bus Request	Jumper Block 1 Settings
7	3	
7	2	
7	1	
7	0	
6	3	
6	2	
6	1	
6	0	
5	3	
5	2	
5	1	
5	0	

Table dev5210–9, VMEbus Interrupt and Bus Request Jumper Settings (J1) (continued)

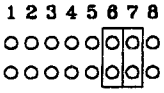
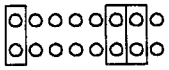
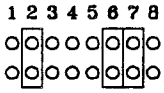
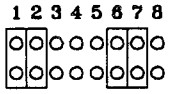
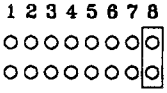
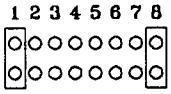
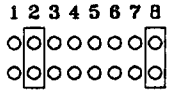
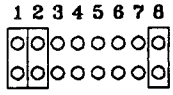
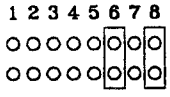
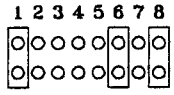
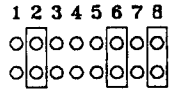
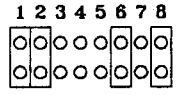
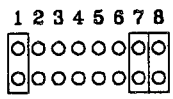
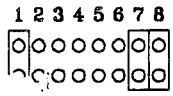
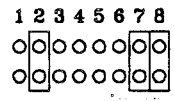
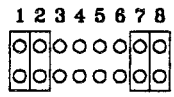
Interrupt Level	Bus Request	Jumper Block 1 Settings
4	3	
4	2	
4	1	
4	0	
3	3	
3	2	
3	1	
3	0	
2	3	
2	2	
2	1	
2	0	

Table dev5210–9, VMEbus Interrupt and Bus Request Jumper Settings (J1) (continued)

Interrupt Level	Bus Request	Jumper Block 1 Settings
1	3	
1	2	
1	1	
1	0	

```
8: Tape Unit Number [0-7,?]                                    (1) ->
```

The STC tape drive interface is a selector type interface (i.e., daisy chained). This entry specifies the tape unit select of the drive to test.

```
    ** Tape Drive models **
1:  Storage Technology Corp. 2921 ..................... MTD-201
2:  Storage Technology Corp. 2922 ..................... MTD-204
3:  Storage Technology Corp. 1963/1968 ................ MTD-202
4:  Fujitsu 2436-L1 ................................... MTD-203

9: Tape Drive Type [1-4,?]                                     (2) ->
```

Enter the menu number that corresponds to the drive type to be tested. Menu entries are listed in the order they appear in the */mnt/bin/lib/DBtapefmt* file.

```
10: Use Standard Defaults for Other Options [y,n,?]            (y) ->
```

A yes answer results in the selection of the default value for all remaining prompts. This prevents having to explicitly enter a RETURN in response to every remaining prompt.

```
   ** Tape Spool Size in Feet **
1:  600 ft.
2: 1200 ft.
3: 2400 ft.
4: 3600 ft.
11: Select Mounted Tape Spool Size [1-4,?]                (1) ->
```

Select the option that corresponds to the tape spool size loaded on the tape drive under test. This option allows limitation of the amount of data written by any subtest, if applicable, to the amount that will fit on the tape. Four tape spool sizes are supported (600 ft., 1200 ft., 2400 ft., and 3600 ft.). Currently, this only applies to the chain mode write/read subtests in the following list:

- 320—Chain mode write (NRZI)
- 321—Chain mode read (NRZI)
- 420—Chain mode write (PE)
- 421—Chain mode read (PE)
- 520—Chain mode write (GCR)
- 521—Chain mode read (GCR)

```
12: Run EOT Sensor Subtest #701 [y,n,?]                   (y) ->
```

This entry specifies if subtest 701, the EOT Sensor test, is executed or not. If a large tape spool is mounted, the EOT subtest can take more than five minutes to execute on some of the larger tape spool sizes.

```
   ** Available Data Transfer VMEbus Address Modifiers **
1:  Standard Supervisory Access (16 bit) (0x3d)
2:  Standard Non-Supervisory Access (16 bit) (0x39)
13: Data Transfer VMEbus Address Modifier [1-2,?]         (1) ->
```

Enter the menu number for the desired VMEbus address modifier to use with all VMEbus data transfers from or to the tape drive. The CONVEX VMEbus subsystem answers to all VMEbus address modifiers. Therefore, this option is likely to have no affect on transfers.

```
 ** Available Tape Velocities (IPS) **
1:   50
2:  100
14: Standard Tape Velocity [1-2,?]                        (2) ->
```

Select the default tape velocity (tape speed in inches per second) to use for all subtests that are not dependent on tape velocity.

```
15: Standard Tape Block Size [16-16777216,?]              (8192) ->
```

The entry specifies the tape block size to use for 90% of the write/read tests (Classes 3, 4, and 5). A size greater than 128 Kbytes results in all standard transfers being performed in data chain mode with a chain interval size of 64 Kbytes. Increasing the size can greatly increase the amount of time required for test execution.

```
16: Large Tape Block Size [262144-16777216,?]        (16777216) ->
```

The entry specifies the tape block size to use for the chain mode write and read subtests. The minimum size is 256 Kbytes. CONVEX UNIX can write tape blocks as long as 16 Mbytes. The maximum size is limited by the amount of contiguous physical memory present in the target system.

```
** Printer On/Off Enable/Disable Options (bit mapped) **
  0x0001: Enable printer ON string before error
  0x0002: Enable printer OFF string after error

17: Select Printer On/Off Mode [0x0-0x3,?]              (0x0) ->
```

This prompt allows a specified character string to be sent to the printer before and/or after an error (and its data) is displayed. Although any string up to 64 characters in length may be specified, the intended use is to selectively turn a printer on before an error is displayed and to turn a printer off after an error has been displayed. This is a paper saving feature when executing *dev5210* multiple times or for long periods of time. This assumes a printer is connected to the auxiliary port on the display terminal where *dev5210* is executing. It also assumes the auxiliary port can be turned on and off via an escape character sequence.

Selection of both options is achieved by entering the hexadecimal mask obtained by ORing the two options together (0x03).

```
18: Printer On Character Sequence (before error)
    [<printer on string>,?]                    (\033[?5i) ->
```

This option allows the specification of the enable printer port escape character sequence. The default value is the "Enter Auto Print Mode" sequence for terminals that support VT100 terminal protocol. Control characters may be specified by using standard C programming style escape sequences. For example:

\033	Octal value of the ASCII escape character (0x1b)
\x1b	Same as above value but specified in hex
\r	Carriage return
\n	Line feed
\t	Tab character
\b	Backspace character
\f	Form feed character

```
19: Printer Off Character Sequence (after error)
    [<printer off string>,?]                          (\033[?4i) ->
```

This option allows the specification of the disable printer port escape character sequence. The default value is the "Exit Auto Print Mode" sequence for terminals that support VT100 terminal protocol. Control characters may be specified by using standard C programming style escape sequences. For example:

\033	Octal value of the ASCII escape character (0x1b)
\x1b	Same as above value but specified in hex
\r	Carriage return
\n	Line feed
\t	Tab character
\b	Backspace character
\f	Form feed character

```
20: Use Standard Debug Setup [y,n,?]                          (y) ->
```

A "**yes**" answer results in the selection of the default value for all debug mode related prompts. This prevents having to explicitly enter a RETURN in response to every remaining prompt.

```
21: Pattern for Write/Read Subtests [<hexadecimal pattern>,?]
                                                        (0x6db6) ->
```

Enter the hexadecimal data pattern to use for all tape write/read subtests. The pattern may be any length from 1 nibble to 256 bytes. The pattern is replicated as necessary when formatting buffers for tape writes.

The pattern can be specified via a file on the SPU disk. For this method enter a "+" followed by the optional filename of the pattern file. If the filename is omitted, the test defaults to the file *dev5210.pat*. The pattern may contain white space and be spread across multiple lines if desired.

> **NOTE**
>
> The buffer fill pattern before any reads is "0x55aa55aaaa55aa55." Therefore, to ensure accurate test results, this pattern should be avoided as the write/read data pattern.

```
22: Maximum Media Error Retry Count [0-999,?]                 (9) ->
```

This entry allows specification of the ***maximum*** number of media type error retries that can occur when attempting to recover from a media error. This is in addition to the original attempt. Therefore, a retry count of 9 results in 10 total ***maximum*** tries of a tape operation. A 0 value causes all media errors to be considered fatal.

```
23: Retry Formatter Correctable Media Errors [y,n,?]      (n) ->
```

Answering "**yes**" or "**no**" to this prompt controls whether or not to retry tape media errors that are correctable by the tape formatter. These can occur on both writes and reads of the tape.

```
  ** Tape Media Error Logging Methods (bit mapped) **
0x0001: After Test Completion
0x0002: After Each Subtest
0x0004: Upon Occurrence (Real time)

24: Select Media Error Logging Method [0x0-0x7,?]      (0x1) ->
```

Select how tape media errors are logged to the display.

> **NOTE**
>
> Selection of the options is achieved by entering the hexadecimal mask obtained by ORing the desired options together. For example, if the first two options are desired, enter **0x3**. If all options are desired, enter **0x7**.

Media errors are isolated into two classes:

- **1**—Formatter correctable errors
- **2**—Uncorrectable errors

Formatter correctable errors are errors that are mathematically correctable by the tape formatter. These can occur on both reads or writes. Uncorrectable errors cannot be corrected by the formatter and must be retried. Both of the error types can be logged as they occur, after each subtest, after the entire test, or after both.

```
  ** Available Data Miscompare Dump Modes **
1: Separate Expected and Actual Values into Two Blocks.
2: Mix Expected and Actual Values (xx/xx).
3: Only Show Bytes that Miscompare.

25: Select Data Miscompare Display Mode [1-3,?]          (2) ->
```

This option specifies the format of data miscompare dumps. Select one of three different styles. The "mixed" mode uses the least amount of display space while the "separated block" mode requires the most. The "show miscompares only" gives greater depth into the data (assuming miscomparisons occur at sparse intervals). A sample of each format's output follows:

```
------------ Separate Expected and Actual Values into Two Blocks ------------
Expected:
    00100000:  6d* b6  6d  b6* 6d  b6  6d  b6* 6d  b6  6d  b6  6d  b6  6d* b6
    00100010:  6d  b6  6d  b6  6d  b6  6d  b6  6d  b6  6d  b6  6d  b6  6d  b6
Actual:
    00100000:  00* b6  6d  77* 6d  b6  6d  88* 6d  b6  6d  b6  6d  b6  99* b6
    00100010:  6d  b6  6d  b6  6d  b6  6d  b6  6d  b6  6d  b6  6d  b6  6d  b6


------------------- Mix Expected and Actual Values (xx/xx) ------------------
Expected/Actual:
    00100000:  6d/00* b6/b6  6d/6d  b6/77* 6d/6d  b6/b6  6d/6d  b6/88*
    00100008:  6d/6d  b6/b6  6d/6d  b6/b6  6d/6d  b6/b6  6d/99* b6/b6


---------------------- Only Show Bytes that Miscompare -----------------------
Expected/Actual (Miscompares only):
    00100000: 6d/00*  00100003: b6/77*  00100007: b6/88*  0010001e: b6/88*
```

```
26: Enter Data Miscompare Line Dump Count [1-1000,?]        (4) ->
```

This option specifies the ***maximum*** number of display lines to use when dumping data after a miscompare occurs.

```
 ** VBTC register dump modes **
1: After Error
2: After Each Command Completion
3: Never

27: Select Controller Register Dump Mode [1-3,?]            (3) ->
```

The register dump mode option allows the last known register state of the VBTC to be displayed after each command completes or after an error occurs. The "After Each Command Completion" mode only works if the "CCU driver single step mode" (show each CCU driver message after it is returned) is selected in the next option.

```
** USER Debug Options (bit mapped) **
  0x0001: Disable Asynchronous Command Mode
  0x0002: Disable Multi-Record Buffering
  0x0004: Disable Reset of Controller After ^C
  0x0008: Disable Hard Error Trapping (logging)
  0x0010: Enter Debugger After an Error Occurs
  0x0100: Pause AFTER each CCU driver command is returned
  0x0200: Show each CCU driver message AFTER it is returned
  0x0400: Pause BEFORE each CCU driver message is sent
  0x0800: Show each CCU driver message BEFORE it is sent

28: User Debug Option Mask [0x0-0xfff,?]                  (0x0) ->
```

These options allow the standard test behavior to be altered in ways that are often useful for troubleshooting. In addition, the test can be paused ***before*** or ***after*** each command (i.e., typically one controller operation) is sent to the CCU driver. The affect of each option is described below in more detail.

NOTE

Selection of the options is achieved by entering the hexadecimal mask obtained by ORing the desired options together. For example, if the first three options are desired, enter **0x7**. If all options are desired, enter **0xfff**.

`0x0001: Disable Asynchronous Command Mode`

This option inhibits the asynchronous command mode used in most of the write/read subtests. Asynchronous command mode occurs when multiple CCU driver commands are transmitted without waiting for a response to the commands. This allows the test to meet the tape drive reinstruct time and keep the tape spinning at maximum velocity by eliminating the 2 μs to 4 μs overhead required to transmit a command and receive its response via MBS. Unfortunately, this can be confusing when using the CCU driver single-step mode. Therefore, this option allows the synchronous command mode to be disabled.

`0x0002: Disable Multi-Record Buffering`

This option inhibits the multirecord buffering that takes place in 75% of the write/read subtests. Multirecord buffering causes the test to write or read as much data as the main memory buffer can hold at once. This allows the test to keep the tape spinning at maximum velocity as long as possible (i.e., the number of tape start/stop cycles is reduced). Unfortunately, this can be confusing when using the register dump on error mode. For example, if 4 blocks are read into the buffer and a data compare error occurs on the first and if the register dump on error mode was set, the register dump would be for the fourth block read ***not*** the first. Therefore, this option forces one read at a time each followed by a data compare.

NOTE

The previous option does not work for all subtests that do multirecord buffering.

`0x0004: Disable Reset of Controller After ^C`

Normally whenever the test is aborted by entering CTRL **C**, the controller is reset. This may destroy valuable register states in some cases. This option prevents the reset from occurring.

`0x0008: Disable Hard Error Trapping (logging)`

By default, this test monitors for ***hard*** system errors and aborts if a hard error occurs. Because hard errors are processed as an interrupt to the normal test logic, the state of the test cannot be reported when a hard error occurs. Since hard errors always result in the immediate halt of the main memory system, a subtest may eventually fail without hard error logging enabled. This is often useful since the subtest state is reported (i.e., more fail data is reported to allow more insight into the possible source of the problem).

`0x0010: Enter Debugger After an Error Occurs`

This option allows automatic entry to the interactive debugger any time an error is detected within a subtest. The debugger may also be invoked by specifying the "***-d***" option at test invocation time (i.e., **dev5210**[x] **-d**).

```
0x0100: Pause AFTER each CCU driver command is returned
0x0200: Show each CCU driver message AFTER it is returned
0x0400: Pause BEFORE each CCU driver message is sent
0x0800: Show each CCU driver message BEFORE it is sent
```

These bit options allows single stepping ***before*** and or ***after*** each CCU driver command. In addition, the internal command can be displayed by selecting one of the "show command" option bits. This is a valuable debugging tool when used with the register dump after each command mode. Also, the main memory read/write buffer and CCU memory can be examined by entering the debugger. See the "Interactive Debugger" section at the end of this test description for more details on the debugger.

For most cases, the ***after*** modes are sufficient. The following list shows the valid responses while paused during the single-step mode:

Space bar	Continue
Return	Continue
:	Enter debugger

```
29: Enter OK, or :NN to return to question NN [OK]        (OK) ->
```

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

Class Descriptions

The *dev5210* test contains the seven classes of subtests listed in the following table:

Table dev5210–10, *dev5210* Test Classes

Class	Description
1	VBTC loopback tests
2	Formatter/drive tests
3	Write/read tests—800 bpi (NRZI)
4	Write/read tests—1,600 bpi (PE)
5	Write/read tests—6,250 bpi (GCR)
6	Exception tests
7	Miscellaneous tests

NOTE

In the previous table, Class 3, 4, and 5 all perform the same subtests but at different recording densities and parameters.

All *dev5210* subtests are loopable under the *dshell*.

Class 1 Subtests

Class 1 subtests only test the VBTC via the VBTC Diagnostic Loopback Mode; no tape drive is required. Class 1 subtests verify the following functionalities:

- The ability to communicate with the VMEbus Input/Output Processor (VIOP), VMEbus Control Unit (VBCU), and the VMEbus Tape Controller (VBTC)
- The ability of the VBTC to interrupt and to mask interrupts
- Accessibility to main memory
- Detection of FIFO parity errors

Most Class 1 subtests use the VBTC Diagnostic Loopback Mode. Diagnostic Loopback Mode is enabled by setting bit <6> in the control register at address 0x*n*01. When the Diagnostic Loopback Mode is enabled, it is verified (upon command termination) by reading the status register at address 0x*n*10. The VBTC is reset at the start of each subtest in this class (except Subtest 101) by writing to the VBTC register at address 0x*n*0F.

The following table lists all Class 1 subtests, their descriptions, and the times required to execute each subtest:

Table dev5210–11, Class 1 Subtests

Subtest	Description	Time (min:sec)
101	VBTC Pending Register RAM Pattern Test	00:07
102	VBTC Reset Test	00:00
103	VBTC Interrupt Loopback Test	00:02
104	VBTC FIFO Pattern Test	00:14
105	VBTC FIFO Variable Size Write/Read Test	01:46

The times listed are only examples. The time required to execute each subtest changes depending on the amount of memory, size of the tape, density, and the velocity of the tape drive.

Subtest 101, VBTC Pending Register RAM Pattern Test

Subtest 101 verifies the integrity of the VBTC pending level registers via pattern tests. Registers from 0x01 through 0x0E are pattern tested using the patterns in the following table:

Table dev5210–12, Subtest 101 Test Patterns

Description	Hexadecimal Pattern	Rotations (Iterations)
Eight zeros and eight ones	0x00ff	2
Walking ones	0x0102040810204080	8
Walking zeros	0xfefdfbf7efdfbf7f	8
Alternating zeros and ones	0xaa55	2
Two ones and a zero	0xdb6db6	3
Two zeros and a one	0x249249	3
Two zeros and two ones	0xcc993366	4

Each byte of each pattern is written to and read from each RAM location. For example, the eight zeros and eight ones pattern (0x00ff) is written to and read from each RAM location once. Then it is rotated (0xff00) and rewritten/read. Each rotation is written, read, and compared twice.

The subtest does not write the start flag or the reset flag. It requires that the VBTC decode addresses on the bus.

Subtest 102, VBTC Reset Test

Subtest 102 verifies that multiple VBTC resets result in the same controller state. This is the first subtest to actually execute a command. This test begins by resetting the VBTC. It then executes a *NOP* command in the Diagnostic Loopback Mode. After the *NOP* command completes (i.e., the controller interrupts), the register state of the controller is saved. The *NOP* command is supervised by a 1-second timeout. The above sequence is then repeated and the ending register state is partially compared with the original register state. Differences are reported if they occur.

Subtest 103, VBTC Interrupt Loopback Test

Subtest 103 verifies that the VBTC command completion interrupts work. Initially the VBTC is reset. Next the subtest verifies that the VBTC can generate a 68020 interrupt on the VIOP. The interrupt capability is tested at the selected VBCU interrupt level and at 68020 interrupt level 3. It also verifies that the interrupt enable bit works by de-asserting it and expecting the driver to get a timeout error while executing a command. A *NOP* command, in Diagnostic Loopback Mode, is used for all commands.

Subtest 104, VBTC FIFO Pattern Test

Subtest 104 verifies the VBTC FIFO via pattern tests in the Diagnostic Loopback Mode. Initially the VBTC is reset. Since the VBTC FIFO cannot be filled (i.e., capacity is 1,024 bytes) in the Diagnostic Loopback Mode, the subtest writes and reads half of the FIFO (512 bytes) with each pattern rotation twice. Due to the way the FIFO works, this tests all FIFO RAM locations. The

patterns in the following table are used:

Table dev5210–13, Subtest 104 Test Patterns

Description	Hexadecimal Pattern	Rotations (Iterations)
Eight zeros and eight ones	0x00ff	2
Walking ones	0x0102040810204080	8
Walking zeros	0xfefdfbf7efdfbf7f	8
Alternating zeros and ones	0xaa55	2
Two ones and a zero	0xdb6db6	3
Two zeros and a one	0x249249	3
Two zeros and two ones	0xcc993366	4

Each byte of each pattern is written to and read from each RAM location. For example, the eight zeros and eight ones pattern (0x00ff) is written to and read from each RAM location once. Then it is rotated (0xff00) and rewritten/read. Each rotation is written, read, and compared twice.

Subtest 105, VBTC FIFO Variable Size Write/Read Test

Subtest 105 verifies the VBTC FIFO via variable length reads and writes. Initially the subtest resets the VBTC. It then writes and reads varying block sizes in the Diagnostic Loopback Mode. Each size is written from both EVEN and ODD addresses. During reads, the controller transfer count is set to 512 bytes more than the current size of the written data. At the end of the read, the VBTC is expected to have a residual transfer count of 512. In addition, data compares occur on the read data and the 512 bytes beyond the read data. The 512 byte overflow buffer beyond the read data is expected to contain the initial buffer fill pattern. All transfer sizes starting with a single byte up to 957 bytes are tried (***even*** and ***odd*** addresses).

Class 2 Subtests

Class 2 contains subtests not specific to tape recording density. No data is actually written to the tape (i.e., the digital loopback write command (*LWR*) is used).

The following table lists all Class 2 subtests, their descriptions, and the times required to execute each subtest:

Table dev5210–14, Class 2 Subtests

Subtest	Description	Time (min:sec)
200	Formatter Accessibility Test	00:00
201	Formatter/VBTC Interface Test	00:02
203	Formatter Looped Write to Read Test	00:03
204	VBTC Piped Write Test	00:04

The times listed are only examples. The time required to execute each subtest changes depending on the amount of memory, size of the tape, density, and the velocity of the tape drive.

Subtest 200, Formatter Accessibility Test

Subtest 200 verifies that the formatter is accessible and can execute a command. This subtest attempts to execute the simplest formatter command available to verify interconnect to the tape drive/formatter. A *NOP* command is used. According to the *STC 2920 Series Maintenance Manual* (StorageTek Interface Specification), a *NOP* results only in the formatter asserted and then deasserting BUSY. No status lines should be changed.

Subtest 201, Formatter/VBTC Interface Test

Subtest 201 verifies the general interface to the formatter. This subtest uses the *DMS, NOP* command sequence available on the STC 2920 Series drives. It verifies that many of the discrete status lines from the drive are physically connected and readable by the VBTC. Refer to the *STC 2920 Series Maintenance Manual* (Chapter 4) for more information. The following table lists the status lines that are tested:

Table dev5210–15, Tested STC Status Lines

TESTED STC INTERFACE SIGNALS				
NOP #	**Description**	**Mnemonic**	**Connector Pin Number**	**Software Dectectable**
1	Online status	ONLS	J6-49	Yes
2	Identification burst status	ID BRST	J6-25	No
3	File protect status	FPTS	J7-27	Yes
4	Rewinding status	REWS	J7-59	Yes
5	Expecting data status	RECV	J6-23	No
6	Operation incomplete status	OP INC	J6-27	Yes
7	Online status	ONLS	J6-49	Yes
8	Tape mark status	TMS	J6-31	Yes
9	Command reject	REJ	J6-33	Yes
10	Overrun status	OVRNS	J6-35	Yes
11	Data check status	DATA CHK	J6-37	Yes
12	EPROM error status	ROMPS	J6-39	Yes
13	Corrected error status	CRERR	J6-41	Yes
14	Online status	ONLS	J6-49	Yes
15	High density status	HDNS	J6-45	No
16	Ready status	RDYS	J6-53	Yes
17	Write status	WRTS	J6-55	Yes
18–53	MUX bytes (0–3) all 9 bits	ERRMX <0..7,P>	J6-<1,3,5,..17>	Yes

NOTE

Subtest 201 is only supported on the STC 2920 Series drives.

Subtest 203, Formatter Looped Write to Read Test

Subtest 203 verifies the data bus interface to the formatter. This subtest first rewinds the tape to BOT (required by the *LWR* command) and then writes ten 16-Kbyte blocks via the *LWR* (digital loopback write command). This verifies the digital data path between the drive analog circuitry and VBTC.

Subtest 204, VBTC Piped Write Test

Subtest 204 verifies that the VBTC can operate in a pipelined mode. This subtest rewinds the tape to BOT (required by the *LWR* command). The *LWR* command is used to verify that the VBTC can pipeline two commands. Twenty *LWR* commands are pipelined with a transfer size of 16 Kbytes.

Class 3, 4, and 5 Subtests

Class 3, 4, and 5 subtests verify that the drive can write and read data to its tape. All of the tape motion type commands are verified. Where applicable, Class 3, 4, and 5 subtests verify the correct state of the drive prior to the actual test logic being executed. A *NOP* command is issued at the start of each test. This is used to set the tape unit select to the correct unit. In the event the drive is in an incorrect state, the subtest is paused and the operator is requested to intervene and place the drive online.

Each subtest pauses for up to 30 minutes while waiting for the drive to come online and ready. Once the drive is online and ready, the *CLR* command is issued followed by a check of the formatter status registers for errors. Most subtests rewind the tape at this point.

> **NOTE**
>
> This diagnostic allows a maximum of 5 minutes for the rewind to complete.

Read and write subtests take advantage of both current tape position and controller state. This implies the position of the tape and the controller status is known at most times. Initially, if the tape position is not known, the tape is rewound. Additionally, the VBTC is reset, if necessary. Written tape blocks contain address information for verification of positional coordinates.

The following table contains the layout of the tape header written at the start of each block:

Table dev5210–16, Tape Header Layout

Field Description	Number of Bytes
Current block number	2
Number of blocks in this file	2
Current file number	2
Total number of files present	2
Size of this block	4
Subtest that wrote this data	2
Checksum of header	2
Total	16

Class 3, 4, and 5 all perform the same subtests but at different densities as follows:

- **3**—Write/read tests (800 bpi (NRZI))

- **4**—Write/read tests (1,600 bpi (PE))
- **5**—Write/read tests (6,250 bpi (GCR))

"Table dev5210–17, Class 3, 4, and 5 Subtests" lists all Class 3, 4, and 5 subtests, their descriptions, and the time required for each to execute. The times listed are only examples. The time required to execute each subtest changes depending on the amount of memory, size of the tape, density, and the velocity of the tape drive. These subtest are numbered between the range of 300–599 (n00–n99). Subtest numbers in these three classes contain a prefix of *n* (as the hundreds digit), which is used to select tape density. The 300 series subtests are for 800 bpi (NRZI) tapes, 400 series for 1,600 bpi (PE) tapes, and 500 series for 6,250 bpi (GCR) tapes.

Table dev5210–17, Class 3, 4, and 5 Subtests

Subtest	Description	Time (min:sec)
*n*00	ID Burst Write Test	00:02
*n*01	ID Burst Read Test	00:03
*n*02	Write Block Test	00:17
*n*03	Read Block Fwd/Bwd Test	01:06
*n*04	Skip Block Fwd/Bwd Test	01:20
*n*05	Erase Gap Test	00:17
*n*06	Write Tape Mark Test	00:12
*n*07	Skip Tape Mark Test	00:14
*n*08	Write Block/Tape Mark Test	00:25
*n*09	Read Block/Tape Mark Fwd/Bwd Test	01:22
*n*10	Skip Block/Tape Mark Fwd/Bwd Test	01:07
*n*11	Write File UNIX Style Test	00:38
*n*12	Read UNIX Style Written File Test	00:48
*n*13	Write Variable Size Blocks Test	00:22
*n*14	Read Variable Size Blocks Test	00:29
*n*20	Chain Mode Write Test	00:23
*n*21	Chain Mode Read Test	00:44
*n*50	Write/Read All Velocities Comb. Test	01:28

[1] *n* varies from 3 to 5: 3 is 800 bpi; 4 is 1,600 bpi; and 5 is 6,250 bpi. The diagnostic defaults to all densities specified in the */mnt/bin/lib/DBtapefmt* file.

Subtest *n*00, ID Burst Write Test

Subtest *n*00 verifies that the drive under test can write an ID burst. This subtest begins by rewinding the tape to BOT. The subtest then writes a tape mark and verifies that no errors occur and that the correct recording density is selected. This verifies that the ID burst was successfully written since any write from BOT causes the ID BURST, for the current recording density, to be written and verified (read after write).

Subtest *n*01, ID Burst Read Test

Subtest *n*01 verifies that the drive under test can read an ID burst. This subtest rewinds the tape to BOT and then issues a Read Forward (*RDF*) command expecting to transfer zero bytes (i.e., a tape mark is detected). In addition, the test verifies that the density reflects the assumed ID

burst that was written by subtest *n*00.

Subtest *n*02, Write Block Test

Subtest *n*02 writes 200 fixed length tape blocks from BOT (i.e., the tape is first rewound). This block size is the block size specified in the "Test Parameter Menu." No tape marks are written during the subtest.

Subtest *n*03, Read Block Fwd/Bwd Test

Subtest *n*03 verifies simple reads. This subtest reads the 200 blocks written by Subtest *n*02. It begins by rewinding the tape to BOT and issuing 200 *RDF* commands. Next, the subtest issues 200 Read Backward (*RDB*) commands. Data compares occur at the end of each read pass.

Subtest *n*04, Skip Block Fwd/Bwd Test

Subtest *n*04 verifies that the Forward Skip Block (*FSB*) and the Backward Skip Block (*BSB*) commands can skip over tape blocks. This test skips over the data written by Subtest *n*02. The tape is rewound initially. After each seek from block to block (using the necessary count of one of the above *FSB* or *BSB* commands), a Read Forward (*RDF*) command is performed and the tape header is checked to verify that a seek error (tape positioning error) has not occurred. The following list contains the order in which the subtest skips and the number of the blocks that it skips:

- Skip forward (further each time) to the following blocks:
  - 2, 4, 8, 14, 22, 32, 64, 128, 200
- Skip backward (further each time) to the following blocks:
  - 198, 196, 192, 186, 178, 168, 136, 72, 1
- Skip forward then backward (sawtooth like pattern) to the following blocks:
  - 90, 102, 92, 104, 94, 106, 96, 108, 98, 110, 100
- Skip backward then forward (sawtooth like pattern) to the following blocks:
  - 110, 98, 108, 96, 106, 94, 104, 92, 102, 90, 100
- Skip backward and forward (accordion like pattern) to the following blocks:
  - 130, 70, 120, 80, 110, 90, 106, 94, 104, 96, 102, 98

Subtest *n*05, Erase Gap Test

Subtest *n*05 verifies that the Erase Gap (*ERG*) command can erase the tape. This subtest begins by rewinding the tape. It then writes 10 blocks and verifies them by reading backwards all 10 blocks. It then positions the tape just beyond the first block with a Backward Space File (*BSF*) command. Next, it erases the second tape block and then rewinds the tape. Since the *ERG* command is supposed to erase approximately 3.5 inches of tape, the length of the blocks written are slightly more than this. The size is, therefore, based on the current recording density. Refer to the following table for the erase gap sizes.

Table dev5210–18, Erase Gap Sizes

Density	Block Sizes (inches)
800 bpi	5.12 inches (4 Kbytes)
1,600 bpi	5.12 inches (8 Kbytes)
6,250 bpi	5.24 inches (32 Kbytes)

Block 1 should not be affected by the erase. Block 2 should be unreadable after the erase. The first block is read and verified. Next, the subtest tries to read the erased block 2. It is possible to get two different outcomes. First, a tape read error may result (most likely). Second, the read may complete successfully if the third block is actually read instead of the second (rare possibility).

Subtest *n*06, Write Tape Mark Test

Subtest *n*06 verifies that multiple tape marks can be written. This subtest begins by rewinding the tape and then writes one block followed by 200 tape marks and then a second block. Both blocks are the size of a tape block header since they are only used to verify tape position.

Subtest *n*07, Skip Tape Mark Test

Subtest *n*07 verifies that multiple tape marks (200 with no data between them) can be skipped over correctly. Also this subtest verifies the tape marks are written correctly. This subtest uses the data written by *n*06. Initially the tape is rewound to BOT. The first block is read and then 200 Forward Skip File (*FSF*) commands are executed. Next, the subtest attempts to read the second block. Tape position is verified by checking the second block's header.

Subtest *n*08, Write Block/Tape Mark Test

Subtest *n*08 verifies that a combination of blocks and file marks can be written. This subtest writes 10 files of 25 blocks, each separated by tape marks. An end of tape mark is written after the last tape mark.

Subtest *n*09, Read Block/Tape Mark Fwd/Bwd Test

Subtest *n*09 verifies that the combination of blocks and file marks written by subtest *n*08 are readable. All of the blocks are read and data compared. In addition, the tape marks are read using the *RDF*, *RDB* command sequence. The data is first read forward and then a data compare is performed. Next, the data is read backward and another data compare is performed. This subtest uses the *RDF* and *RDB* commands.

Subtest *n*10, Skip Block/Tape Mark Fwd/Bwd Test

Subtest *n*10, verifies that the File Skip Forward/Backward commands. The the Forward Skip Block (*FSB*), Backward Skip Block (*BSB*), Forward Skip File (*FSF*), and the Backward Skip File (*BSF*) commands are used. This test skips over the data written by subtest *n*08. The tape is

rewound initially. After each seek from point to point (using the necessary combination of the above commands), a Read Forward (*RDF*) is performed and the tape header is checked to verify that a seek error (tape positioning error) has not occurred. The block/file coordinates that the test skips to are listed in the following list; in each case the first number listed is the file number and the second number is the block number:

- Skip forward (further each time) to {file, block}
  - {2, 1}
  - {5, 1}
  - {10, 1}
- Skip backward (further each time) to {file, block}
  - {8, 24}
  - {4, 24}
  - {1, 24}
- Skip backward and forward (accordion like pattern) to {file, block}
  - {2, 10}
  - {1, 2}
  - {9, 23}
  - {7, 24}
  - {4, 1}
  - {10, 25}

Subtest *n*11, Write File UNIX Style Test

Subtest *n*11 verifies that a file can be written as the CONVEX UNIX driver writes files. This subtest writes several files using the same command sequence as the CONVEX UNIX driver. The sequence for each file is:

1. *N* write-blocks
2. Write-tape mark
3. Write-tape mark
4. Backspace-file

Asynchronous I/O is used for the entire command stream to the CCU driver. The number of blocks per file and the file count varies with the recording density. Refer to the following table for the block count and file count:

Table dev5210–19, Subtest *n*11 Write File/Block Count

Density	Block Count (*N*)	File Count
800 BPI	8	8
1,600 BPI	16	16
6,250 BPI	50	20

Subtest *n*12, Read UNIX Style Written File Test

Subtest *n*12 verifies that the file written by subtest *n*11. The subtest rewinds the tape initially and then reads all of the tape blocks and marks written by subtest *n*11.

Subtest *n*13, Write Variable Size Blocks Test

Subtest *n*13 verifies that the variable length tape blocks can be written. This subtest writes varying block sizes starting with 1 byte (in increments of one) up to 258 bytes and then -2 thru +2 around every base 2 boundary up to 2^{16} (64 Kbytes) (i.e., 510–514, 1022–1026). Tape headers are only written if the current block size is large enough to contain the entire header.

Subtest *n*14, Read Variable Size Blocks Test

Subtest *n*14 verifies that the variable length tape blocks can be read. This subtest reads varying block sizes (written by the subtest *n*13) starting with 1 byte (in increments of one) up to 258 bytes and then -2 thru +2 around every base 2 boundary up to 2^{16} (64 Kbytes) (i.e., 510–514, 1,022–1,026). Tape headers are only read and verified if the current block size is large enough to contain a tape header.

Subtest *n*20, Chain Mode Write Test

Subtest *n*20 writes one ***long gapless*** tape block after rewinding the tape to BOT. The VBTC data chaining mode is used to write the block. The chain interval size is 32 Kbytes. Normally the CCU driver would default to 64 Kbyte intervals (128 Kbyte windows). The actual size of the block written by the test is controlled first by the size of the "Large Tape Block Size" specified in the "Test Parameter Menu". The size is reduced (if necessary) to the maximum size that can be written in the current density on the currently mounted tape spool.

Subtest *n*21, Chain Mode Read Test

Subtest *n*21 verifies that chain mode reads execute properly under a variety of conditions. This subtest reads the data written by subtest *n*20 and performs a data compare. Refer to subtest *n*20 for a description of the subtests algorithm.

Subtest *n*50, Write/Read All Velocities Comb. Test

Subtest *n*50 writes 50 blocks delimited by two tape marks in each velocity and reads back each written group in every other available velocity.

Class 6 Subtests

Class 6 subtests verify that the VBTC and tape formatter can detect and recover from a variety of error conditions. The initial setup at the start of each test is the same as that described for the Class 3, 4, and 5 subtests (i.e., check for online, *CLR*, and rewind). The following table lists all Class 6 Subtests, their descriptions, and the times required to execute each subtest.

Table dev5210–20, Class 6 Subtests

Subtest	Description	Time (min:sec)
600	VBTC Read Underrun Test	00:08
601	VBTC/Drive Forced Parity Error Test	00:03
602	VBTC Chain Mode Missed Interrupt Test	00:10
603	VBTC Chain Mode Read Underrun Test	00:05
604	VBTC Pipe Mode Error Test	00:06
606	VBTC Bus Error Recovery Test	00:23

The times listed in the previous are only examples. The time required to execute each subtest changes depending on the amount of memory, size of the tape, density, and the velocity of the tape drive.

Subtest 600, VBTC Read Underrun Test

Subtest 600 verifies that the VBTC detects a read underrun condition and correctly handshakes for and drops the remaining data. This subtest begins by writing three 16 Kbyte tape blocks from BOT. Two delimiting tape marks are then written. Next, the tape is rewound. Each of the three blocks are read back with transfer counts less than their size (i.e., should cause read underrun). At the end of each read, it is verified that only a read underrun is reported by the VBTC (i.e., no formatter reported errors). Although no data compare occurs, the read tape block headers are verified. After the read of the third block, the test attempts to read across the two trailing tape marks.

Subtest 601, VBTC/Drive Forced Parity Error Test

Subtest 601 verifies that parity errors are detectable. This subtest begins by rewinding the tape to BOT (required by the *LWR* command). It then writes four 4 Kbyte blocks via the *LWR* command with good parity. Next, the test repeats the above write command sequence with bad parity forced by the VBTC. After each *LWR* command the test checks for a drive reported error (parity or data check). The expected error type is controlled by one of the personality bits in the drive database file (*/mnt/bin/lib/DBtapefmt*). Next, an optional drive reset may occur (based on another one of the personality bits in the drive database file) since some drives may not clear a parity error until after a reset. Finally, the *CLR* command is used to insure the previous error state can be cleared.

Subtest 602 VBTC Chain Mode Missed Interrupt Test

Subtest 602 verifies that the VBTC when an interrupt receives late service in the data chain mode. This subtest rewinds the tape to BOT (required by the *LWR* command). It then uses the *LWR* command to verify that the VBTC halts when command chaining is active and a chain interval interrupt is not serviced before the next interval interrupt arrives. The test begins by starting a 128 Kbyte write in data chain mode with an interval size of 16 Kbytes. It then pauses on the third interval for two seconds and expects the VBTC to halt with the appropriate error status. The process is repeated on the fourth, fifth, and sixth chain intervals.

Subtest 603, VBTC Chain Mode Read Underrun Test

Subtest 603 verifies that read underrun is detected in the data chain mode under a variety of boundary conditions. This subtest rewinds the tape to BOT and then writes two 40,960-byte tape blocks (8,192 * 5) followed by two tape marks. The tape is then rewound and a read with a size of 28,672, followed by a size of 36,864. Both of the reads should cause a read underrun to occur. In addition, the VBTC should continue to read the data until the real end of block is detected. This means the only error that should be indicated in the terminating status is a read underrun. The above read sizes cause the read underrun to occur once on Buffer A and once on Buffer B. Although the data chain mode bit is already reset when read underrun occurs, the subtest still tries to assure it can be detected at the end of a data chain mode transfer (on both Buffer A and Buffer B).

Subtest 604, VBTC Pipe Mode Error Test

Subtest 604 verifies that the VBTC halts command pipelining when an error occurs during piped commands. This subtest begins by rewinding the tape. It then writes a 32 Kbyte block, rewinds the tape, and writes a 16 Kbyte block. This guarantees a read (after the 16 Kbyte block is written) generates an error since there is no preamble lead-in into what appears to be the second block. Next, a *RDF, REW* command sequence is pipelined. The rewind should not execute since *RDF* fails and the VBTC should halt pipelining. The fact that the pended *REW* command did not execute should be indicated by the Command Abort status bit being asserted by the VBTC. In addition, BOT should not be present after the failure (i.e., make sure the *REW* command was not executed).

Subtest 606, VBTC Bus Error Recover Test

Subtest 606 verifies that VMEbus errors are recoverable. Initially, the tape is rewound to BOT. The subtest then writes four 4,096-byte tape blocks with a VMEbus standard address of 0xc00000 (bits <22> and <23> set). The above address is not mapped by the VBCU and should result in a VMEbus bus error. The test verifies that the VBTC reports a bus error after each write.

Class 7 Subtests

Class 7 consists of the tape velocity measurement subtest and the end of tape sensor subtest. Both of these subtests have initialization sequences similar to Classes 3-6. The following table lists all Class 7 Subtests, their descriptions, and the times required to execute each subtest.

Table dev5210–21, Class 7 Subtests

Subtest	Description	Time (min:sec)
700	Drive Tape Velocity Verification	00:39
701	Drive EOT Sensor Verification Test	01:20

The times listed in the previous table are only examples. The time required to execute each subtest changes depending on the amount of memory, size of the tape, density, and the velocity of

the tape drive.

Subtest 700, Drive Tape Velocity Verification

Subtest 700 verifies that all available tape velocities on the current drive in all supported densities. The subtest verifies that the achieved tape velocity is within the specified tolerance (in the database file */mnt/bin/lib/DBtapefmt*). Suggested (and current) tolerance is ± 5%. The subtest verifies that each velocity can be selected via software control (whatever the method). The subtest starts with the lowest tape density and ends on the most dense recording format while verifying every available velocity. For each density and velocity the subtest rewinds the tape and then writes enough data to keep the tape moving for a minimum of 4 seconds. The subtest determines the number of blocks needed to meet the 4-second time requirement. The following table lists the block sizes used for each density:

Table dev5210–22, Block Sizes Written

Density	Block Sizes
800 bpi	64 Kbytes
1,600 bpi	128 Kbytes
6,250 bpi	512 Kbytes

The time required to write the first block is ignored to get the tape up to speed and to write the ID burst. The time required to write the remaining blocks is measured and the resulting tape velocity in Inches Per Second (IPS) is calculated and displayed in the following format:

```
Density ---- Velocity Nom/Meas ---- Tolerance ---- Delta
PE              50.0 /  49.8         +/-5.0%       -0.4%
PE             100.0 /  99.4         +/-5.0%       -0.6%
GCR             50.0 /  50.0         +/-5.0%        0.0%
GCR            100.0 / 100.1         +/-5.0%       +0.1%
```

Subtest 701, Drive EOT Sensor Verification Test

Subtest 701 verifies that EOT can be sensed by writing until EOT is detected. This subtest rewinds the tape to BOT and continues to write 8 Kbyte blocks until EOT is sensed. It is probable that the tape will go off the spool if EOT is not sensed.

Interactive Debugger

The diagnostic provides an interactive debugger that supports the ability to execute commands from a script file. This allows more debug flexibility. Invocation of the debugger is achieved by one of the three following methods:

- Use the **-d** option when invoking the diagnostic (enter **dev5210**[x] **-d**). No subtests are executed and the debugger is invoked.

- The prompt "`User Debug Option Mask [0x0-0xfff,?]`" provides a bit option to force the diagnostic to enter the debugger after an error is reported. To ensure that this option is set, **0x10** must be ORed into the hexadecimal bit-pattern response for the prompt.
- Enter a ":" when in single-step mode.

Once the interactive debugger is entered, online help commands are available. By entering **help**, the following screen is displayed:

Figure dev5210–6, Interactive Debugger On-line Help

```
Input base specification:
    0dNN - decimal,  0xNN or NN - hexadecimal,  the default is hexadecimal

Meta-command sequences:
   ![UNIX_CMD]       - execute UNIX_CMD
   !![UNIX_CMD]      - fork a shell and execute UNIX_CMD (allows redirection)
   <FILE             - redirect input from FILE (recursive)
   <<FILE            - end input from current file and change input to FILE

Commands:
    Commands may be abbreviated as long as the abbreviation is unique.

    help    [COMMAND ...]                    - display general or specific help
    buffer                                   - display main memory buffer data
    cd      [DIRECTORY]                      - change to DIRECTORY
    pause   [-n] [seconds]                   - pause for <C/R> or seconds
    quit                                     - exit debug mode
    skip    [-d dbg_mask] [-emq] [count]     - set single step skip mode/count
    mb      begin [end]                      - modify/[dump] bytes (VIOP)
    mw      begin [end]                      - modify/[dump] words (VIOP)
    ml      begin [end]                      - modify/[dump] longs (VIOP)
    fb      begin [end] value [incr [step]]  - fill bytes (VIOP)
    fw      begin [end] value [incr [step]]  - fill words (VIOP)
    fl      begin [end] value [incr [step]]  - fill longs (VIOP)
    mmb     begin [end]                      - modify/[dump] bytes (Main mem)
    mmw     begin [end]                      - modify/[dump] words (Main mem)
    mml     begin [end]                      - modify/[dump] longs (Main mem)
    mfb     begin [end] value [incr [step]]  - fill bytes (Main mem)
    mfw     begin [end] value [incr [step]]  - fill words (Main mem)
    mfl     begin [end] value [incr [step]]  - fill longs (Main mem)
    reg                                      - display current VBTC registers
    reset                                    - reset VBTC/tape drive
```

In addition to the help screen in the previous figure, help for each specific command is obtained by entering:

help *command*

In the previous sequence, replace *command* with the desired debugger command. Abbreviations of the desired commands may be used. For example, for help with all commands that start with the letter "r," enter:

help r

Interactive Debugger Command Descriptions

help

Usage: **help** [COMMAND ...]

Displays general or specific help, where COMMAND is replaced with the desired interactive debugger command. Specific help is displayed for COMMAND. The COMMAND may be an abbreviation. The following example would list help for all commands that start with the letter "r":

help r

buffer

Usage: **buffer**

Displays main memory buffer address and length.

cd

Usage: **cd** [PATH]

Changes to desired directory, where PATH may be any valid directory path. If PATH is omitted, the default path is $HOME or / if $HOME not set.

pause

Usage: **pause** [-n] [seconds]

Wait for specified amount of time or for a RETURN if the time is omitted, where:

-n means do not echo the pause message

seconds specifies the number of seconds to pause

quit

Usage: **quit**

Typing **quit** exits the interactive debugger.

skip

Usage: **skip** [-d MASK] [-emq] [COUNT]

Set the single step skip count where:

-e Skip until CCU driver returns an error (non-zero in the status field).

-m Same as -e, except non-fatal media errors are NOT stopped on.

-q Disable printing while in skip mode. This will cause the test to "skip pause points" at normal execution speed since nothing will be printed (i.e., no pause messages).

COUNT Skip the next COUNT (or 1 if COUNT omitted) single step pause points. If a COUNT is specified with the -e or -m option, the test will skip the next COUNT errors before pausing.

-d MASK Set debug mask to MASK. The debug bit definitions follow:

** USER Debug Options (bit mapped) **
0x0001: Disable Asynchronous Command Mode
0x0002: Disable Multi-Record Buffering
0x0004: Disable Reset of Controller After ^C
0x0008: Disable Hard Error Trapping (logging)
0x0010: Enter Debugger After an Error Occurs
0x0100: Pause AFTER each CCU driver command is returned
0x0200: Show each CCU driver message AFTER it is returned
0x0400: Pause BEFORE each CCU driver message is sent
0x0800: Show each CCU driver message BEFORE it is sent

mb, mw, ml

Usage: **mb begin** [end] [step]
mw begin [end] [step]
ml begin [end] [step]

Displays or modifies, or both, CCU address space in byte-at-a-time mode (mb), word-at-a-time mode (mw), or long-word-at-a-time mode (ml), where:

- **begin** is the initial address
- **end** is the ending address (optional)
- **step** is the address increment (optional (default is access size))

If the ending address is omitted, this command enters an interactive mode that allows modification of memory. The following list gives the valid responses while in interactive mode:

[<value>]	write optional <value> to current address, advance to next address
[<value>]=	write optional <value> to current address, and stay at the present address (re-read)
[<value>]^[N]	write optional <value> to current address, move to address N (address 0 if N is omitted)
[<value>]+[N]	write optional <value> to current address, advance to the next address (N addresses if N is specified)
[<value>]-[N]	write optional <value> to current address, back up to the previous address (N addresses if N is specified)
[<value>]q	write optional <value> to current address, exit interactive mode

Multiple commands may be specified on the same line. A comma or space may be used to separate the commands or value as shown in the following example:

```
Debug mode -> mb c03fc1
<CCU:c03fc1> = 1c 00=ff,1q
```

Where: **1c 00=ff,1q** is an example of executing multiple commands on the same line. This sequence modifies the byte at address 0xc03fc1 to 0, re-reads and displays the new value, modifies the byte to 0xff, skips to address 0xc03fc2 and modifies it to a 0x1, and then quits interactive mode.

fb, fw, fl

Usage: **fb begin** [end] **value** [incr [step]]
fw begin [end] **value** [incr [step]]
fl begin [end] **value** [incr [step]]

Fills memory with specified pattern in byte-at-a-time mode (fb), word-at-a-time mode (fw), or longword-at-a-time move (fl), where:

- **begin** is the starting address
- **end** is the ending address
- **value** is the initial fill value
- **incr** is the fill value increment
- **step** is the address increment

mmb, mmw, mml

Usage: **mmb begin** [end] [step]
mmw begin [end] [step]
mml begin [end] [step]

Displays and or modifies main memory address space in byte-at-a-time mode (mmb), word-at-a-time mode (mmw), or long-word-at-a-time mode (mml), where:

- **begin** is the initial address
- **end** is the ending address (optional)
- **step** is the address increment (optional (default is access size))

If the ending address is omitted, this command enters an interactive mode that allows modification of memory. The following list gives all valid responses while in interactive mode:

[<value>]	write optional <value> to current address, advance to next address
[<value>]=	write optional <value> to current address, and stay at the present address (re-read)
[<value>]^[N]	write optional <value> to current address, move to address N (address 0 if N is omitted)
[<value>]+[N]	write optional <value> to current address, advance to the next address (N addresses if N is specified)
[<value>]-[N]	write optional <value> to current address, back up to the previous address (N addresses if N is specified)

[<value>]q write optional <value> to current address, exit interactive mode

Multiple commands may be specified on the same line. A comma or space may be used to separate the commands or values as shown in the following example:

```
Debug mode -> mmb c03fc1
<Main-Mem:c03fc1> = 1c 00=ff,1q
```

Where: **1c 00=ff,1q** is an example of executing multiple commands on the same line. This sequence modifies the byte at main memory address 0xc03fc1 to 0, re-reads and displays the new value, modifies the byte to 0xff, skips to address 0xc03fc2 and modifies it to a 0x1, and then quits interactive mode.

mfb, mfw, mfl

Usage: **mfb begin** [end] **value** [incr [step]]
mfw begin [end] **value** [incr [step]]
mfl begin [end] **value** [incr [step]]

Fills main memory with specified pattern in byte-at-a-time mode (mfb), word-at-a-time mode (mfw), or longword-at-a-time move (mfl), where:

- **begin** is the starting address
- **end** is the ending address
- **value** is the initial fill value
- **incr** is the fill value increment
- **step** is the address increment

reg

Usage: **reg**

Display current VBTC register state. This command reads the VBTC registers and displays the entire register image in an easily readable format.

reset

Usage: **reset**

Reset the VBTC controller and its attached drive(s) by writing (ORing) a one into the Reset Register at address offset 0xf. Then reset the one by ANDing with 0xfe.

Error Messages

The diagnostic reports four categories of errors:

- Tape positioning errors
- Register mismatch errors

- Data compare errors
- Media errors (not fatal in most cases)

> **NOTE**
>
> There are two type of media errors. Formatter corrected errors are media errors that were mathematically corrected by the tape formatter. These can be ignored or retried based on selected options from the test parameters. Uncorrectable media errors are errors that cannot be corrected by the formatter and must be retried or ignored.

In all cases, the diagnostic returns as much information as possible. The format of the first three types of error messages (tape positioning, register mismatch, and data compare) are basically consistent.

In the following examples, `exp` refers to the expected value, `act` refers to the actual value, `dc` refers to the insignificant bits (don't care bit mask). Also, `diff` is the difference between the actual value and the expected value excluding the insignificant bits. The `diff` value is obtained by ANDing the actual value with the complement of the insignificant bits (don't care bit mask) and exclusive ORing the result with the expected value. All bits that are in discrepancy are set. For example:

```
exp/act/dc = 0x0000/0x0100/0x0000, diff = 0x0100
```

The following figures show examples of all four types of messages:

Figure dev5210–7, Tape Positioning Error Example

```
*****  Mon Mar 27 09:30:37 1989  *****
Test:    dev5210.t  1.1    Class: 5     Subtest: 504 1.1   Count: 1  Error: 7
Failed:  GCR: Skip Block Fwd/Bwd Test

       ---------------- trace point: 504.115.20 ----------------
Tape Position:      File 1 of 1, Block 1 of 200
Current Action:     Verifying the positional coordinates of the tape are as
                    expected.
Other Info:         Error occurred while skipping in the backward direction
                    from block 73 to block 1.  There were 17 successful skips
                    completed prior to the error.
Error Description: The read tape block header indicates a tape positioning
                    error has occurred (i.e., a seek error).
Tape Block Header Mismatch:
          Block-num Block-cnt File-num  File-cnt  Block-size    Wrt-Subtest
exp/act = 0001/0002 00c8/00c8 0001/0001 0001/0001 002000/002000 502
```

NOTE

In the following example, the bytes that miscompare are marked by an asterisk (*).

Figure dev5210–8, Data Compare Error Example

```
*****  Mon Mar 27 09:50:27 1989  *****
Test:    dev5210.t  1.1    Class: 1    Subtest; 105 1.1   Count: 1   Error: 7
Failed:  VBTC FIFO Variable Size Write/Read Test

         ---------------- trace point: 105.125 -----------------
Iteration:          Loop 1 of 1914
Current Action:     Comparing the buffer fill pattern with the data beyond the
                    expected read area.
Other Info:         The failure occurred with a transfer size of 1 and began on
                    an EVEN address.  Transfer sizes from 1 through 957 were
                    being tested on both EVEN and ODD addresses.
Error Description: Data compare error occurred.
                    A data compare error occurred at byte offset 1 (0x1) in the
                    data block under compare.  The data block begins at main
                    memory address: 0x2002000 and is 1 bytes in length. It is
                    in NORMAL order.  The error was in the 512 byte overflow
                    space (at byte offset 0 (0x0) beyond the end of the read
                    data).
Expected/Actual:
    02002001: aa/33* 55/55  aa/aa  aa/aa  55/55  aa/aa  55/55  55/55
    02002009: aa/aa  55/55  aa/aa  aa/aa  55/55  aa/aa  55/55  55/55
    02002011: aa/aa  55/55  aa/aa  aa/aa  55/55  aa/aa  55/55  55/55
    02002019: aa/aa  55/55  aa/aa  aa/aa  55/55  aa/aa  55/55  55/55
```

Figure dev5210–9, Register Mismatch Error Example

```
*****  Mon Mar 27 09:50:27 1989  *****
Test:    dev5210.t  1.1    Class: 2    Subtest; 201 1.1   Count: 1   Error: 7
Failed:  Formatter/VBTC Interface Test

         ---------------- trace point: 201.145 ------------------
Current Action:     Attempting to execute a tape formatter NOP command.
                    The STC Mnemonic of the interface signal that was under
                    test was "ERRMX-0".  This signal is located on connector
                    J6, pin 3.  the multiplex select lines were assumed to be
                    in the following state: SLX[2-0]=0x0.  SLX lines 2-0 are on
                    connection J7, pins 47, 43, and 41, respectively.
                    This failure occurred at NOP number 18 of the DMS/NOP
                    command sequence.  See the STC 2920 series maintenance
                    manual (Ch4) for more info.
Error Description: The VBTC register state at completion of the last command
                    did not match the expected register state.
VBTC Register mismatches:
    3fe[5-4] (mux2):  exp/act/dc = 0x0000/0x0100/0x00, diff = 0x0100
```

Figure dev5210–10, Media Error Example

```
                    ---- TEST MEDIA ERROR TOTALS ----

Media Error Class ---- Total ---- NOT Recovered ---- Recovered ---- Ignored
Formatter-Corrected       13                  0              0           13
Uncorrectable              0                  0              0            0
```

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dev5300

VMEbus Async Controller Test

Overview

This diagnostic provides a functional test for the CONVEX VMEbus Async (68020 based) TTY/Printer Controller (part number 410-001193-200) and its ability to operate in the CONVEX VMEbus I/O environment. The diagnostic verifies the supported controller commands. In addition to the diagnostic subtests within *dev5300*, EPROM self-tests are performed every time the controller is reset or powered on. The EPROM self-tests are described herein.

A VMEbus Async Controller and panel are required; loopback cables (Systech loopback cable – CONVEX part number 603-030012-200) are required if the external loopback serial device tests are to be executed. The diagnostic also provides a debug monitor similar to *vioputil*, which can be enabled on errors or may be invoked from the Service Processor Unit (SPU) prompt. Refer to the "Debug Monitor" section within this test description for more information.

The VMEbus Input Output Processor (VIOP) uses the Event Governed Operating System (EGOS). Service Processor/VIOP communication is accomplished via the Message Based System (MBS) as used by ConvexOS. The Service Processor Unit (SPU), SPU peripherals, main memory subsystem, VIOP, and VMEbus Control Unit (VBCU) are all assumed to be fault free prior to the execution of this diagnostic. Although there are diagnostic messages generated by faults in these subsystems, it is not the intent of this diagnostic to test these subsystems.

Related Documents

This test description is intended as a reference for users who are familiar with the VIOP, VBCU, VMEbus, and the CONVEX I/O system. The user should also be familiar with RS-232 serial devices, Direct Memory Access (DMA) operations and the 68020 microprocessor. Additional information on the VMEbus Async Controller can be found in the following CONVEX documents (part numbers are listed if available):

- IOP Hardware Specification
- VME IOP Difference Document
- VBCU Hardware Specification
- VME Async/Printer Controller Functional Hardware Specification (CONVEX part number 410-001193-000)
- VME Gate Array Functional Specification (CONVEX part number 182-000135-000)

Prerequisites

The following table lists the required hardware depending on the type of machine under test:

Table dev5300–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
VIOP	VIOP
VBCU	PIA
	VBCU

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Test Invocation

The *dev5300* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev5300* test, use the procedure shown in the following figure.

Figure dev5300–1, Initial Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
:test dev5300 [-c [class number(s)]] [-s [subtest number(s)]] RETURN
```

All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

NOTE

Use the previous test invocation sequence for the initial invocation of *dev5300* or for when the state of the machine is unknown. Also, the previous invocation sequence should be used if any hard errors have occurred since the last system initialization.

> **NOTE**
>
> After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev5300** executes all *dev5300* subtests sequentially. To execute a specific class(es) of subtest(s) or one or more individual subtests use the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual.

The following list defines the dash options ([-*option*]):

-f *filename* Use *filename* as the parameter save file. If this option is omitted, the parameter file used is */tmp/dev5300.tmp*.

-d Go to debug mode only; no tests are executed

-V Print the version (build date) of this test

> **NOTE**
>
> The following alternate test invocation procedure is optimal when invoking *dev5300* multiple times. Using this invocation sequence insures that the test is invoked and executed with all of the set-up parameters supplied when the test was last executed with the initial invocation sequence.

Figure dev5300–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
: test dev5300x [-c [class number(s)]] [-s [subtest number(s)]] RETURN
```

The only difference in this alternate invocation sequence is the **x** after **dev5300**. When invoking *dev5300* in this manner, no prompts are displayed. The diagnostic obtains all prompt information from the parameter file created when the initial invocation sequence was performed. Also note that **mminit -s** is only required if the state of the machine is unknown or if hard errors have occurred since the last system initialization.

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows ***all*** prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )).

Figure dev5300–3, Test Parameter Menu

```
Test 'dev5300.t'              Fri Nov 10 15:11:04 1989

                        ENTER TEST PARAMETERS

        []      Encloses allowed input ranges or values
        ()      Encloses the default value
        ^       Returns to the previous prompt
        :nn     Returns to the prompt # nn
        :       Returns to the first unsatisfied prompt
        :?      Reviews previous entries
        ?       Provides specific help where available

 1: Select ioconfig file [<filepath>,?]          (/ioconfig) -> RETURN

      PERIPHERAL CONFIGURATION DATA
     CCU    Chassis   Type     CSR    Int
    -------- ------- -------- ------ ---
 1) viop  7     0    ACM-201  0x03c0  7
 2) viop  5     1    ACM-201  0x03c8  6
 3) viop  5     0    ACM-201  0x1100  1

          *** Enter 0 for manual configuration ***

 2: Ioconfig File Unit to Test [1-3,0,?]                (1) -> 1
 3: VIOP Number [3-7,?]                                 (7) -> 7
 4: VME Chassis Number [0-1,?]                          (0) -> 0
 5: CSR of the Controller [0x10-0xffff,?]          (0x03c0) -> 0x03c0
 6: Interrupt Number of the Controller [1-7,?]          (7) -> 7
     Baud Rate Choices:
         8000=  50       4000=  75
         2000=  110      1000=  134.5
         0800=  150      0400=  200
         0200=  300      0100=  600
         0080=  1050     0040=  1200*
         0020=  2000     0010=  2400*
         0008=  4800     0004=  9600*
         0002=  19200*   0001=  38400*
 7: Select Baud Rates Mask (* indicates default) [0x0-0xffff,?]
                                                    (0x57) -> 0x57
```

Figure dev5300–3, Test Parameter Menu (continued)

```
 8: Port Test Mask (hex), bit 2^n for port n [0x0-0xffff,?]
                                                  (0xffff) -> 0xffff
 9: Enable Debug Monitor [y,n,?]                      (n) -> n
10: Use Defaults for Remaining Parameters [y,n,?]     (y) -> n

  ** Printer On/Off Enable/Disable Options (bit mapped) **
    0x0001: Enable printer ON string before error
    0x0002: Enable printer OFF string after error

11: Select Printer On/Off Mode [0x0-0x3,?]          (0x0) -> 0x3
12: Enable External Loopback Tests [y,n,?]            (n) -> y
13: Ignore Errors [y,n,?]                             (n) -> n
14: Select Download File [<filepath>,?]     (dev5300.xx0) -> dev5300.xx0
     Printer Type Choices:
           Data Products - 0
           Centronics    - 1
15: Select Printer Type [0x0-0x1,?]                 (0x1) -> 0x1
16: Select Pattern File for Printer Test [<filepath>,?]
                                            (dev5300.pat) -> dev5300.pat
17: Select Number of Characters per Line [1-132,?]   (80) -> 80
18: Add <LF> after Line [y,n,?]                       (y) -> y
19: Add <CR> at end of Line [y,n,?]                   (y) -> y
20: Select number of Lines per Page [1-60,?]         (60) -> 60
21: Select Number of Lines to Print [1-1000,?]       (61) -> 60
22: Enter OK, or :NN to return to question NN [OK]   (OK) -> OK
```

Some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. The numbers displayed on the screen during testing may not correspond to those shown in the example "Test Parameter Menu," as the questions illustrated are examples only.

If **OK** or RETURN is entered in response to the last prompt, the test parameter menu terminates and all inputs are no longer changeable.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev5300–2, Getting Help During Test Parameter Entry

Character	Description
:?	Reviews previous entries
?	Provides specific help where available

After the desired help information displays, the system redisplays the last prompt.

When all prompts are answered, the screen displays a TEST PARAMETER SUMMARY which displays the prompts that were answered and their responses. The following figure illustrates an example TEST PARAMETER SUMMARY screen. The actual values and responses vary according to the input.

Figure dev5300–4, Sample Test Parameter Summary

```
                    TEST PARAMETER SUMMARY

Select ioconfig file                                    : ioconfig
Ioconfig File Unit to Test                              : 0
VIOP Number                                             : 7
VME Chassis Number                                      : 0
CSR of the Controller                                   : 0x03c0
Interrupt Number of the Controller                      : 7
Baud Rates Selected:
        1200    2400     9600    19200
        38400
Select Baud Rates Mask (* indicates default)            : 0x57
Port Test Mask (hex), bit 2^n for port n                : 0xffff
Enable Debug Monitor                                    : n
Use Defaults for Remaining Parameters                   : n
Select Printer On/Off Mode                              : 0x0000
Printer On Character Sequence (before error)            : \033[?5i
Printer Off Character Sequence (after error)            : \033[?4i
Enable External Loopback Tests                          : n
Ignore Errors                                           : n
Select Download File                                    : dev5300.xx0
  Printer Type Selected:  Centronics
Select Printer Type                                     : 0x1
Select Pattern File for Printer Test                    : dev5300.pat
Select Number of Characters per Line                    : 80
Add <LF> after Line                                     : y
Add <CR> at end of Line                                 : y
Select number of Lines per Page                         : 60
Select Number of Lines to Print                         : 61
Enter OK, or :NN to return to question NN               : OK
```

Initialization Sequence for *dev5300*

After the last prompt is entered, and before subtest code execution, the following events occur:

- The diagnostic determines if the test was invoked for quick start-up (i.e., **dev5300x**). If so, the diagnostic reads the test parameters from the specified parameter file (default parameter file is */tmp/dev5300.tmp*). If not, the input to the parameters are written to the parameter file (default or user specified).
- The diagnostic checks to see if the Channel Control Unit (CCU) is already loaded with the *dev5300* CCU driver. If the driver is not loaded, the CCU is loaded. After the load completes, the driver is configured for EGOS and then the EGOS probe message starts the driver.

> **NOTE**
>
> The file */mnt/boot_db* is used to determine what memory is installed. If this file is non-existent, it can be created with the command: **scn_util -b > /mnt/boot_db** from the **(spu)>** prompt.

After all the above events have occurred, the test code is started.

Prompt Explanations

The test parameter prompts are repeated and explained in the following paragraphs.

```
1: Select ioconfig file [<filepath>,?]                (/ioconfig) ->
```

This option allows specification of an alternate */ioconfig* file. The file must still be in the same format as a conventional */ioconfig* file.

```
        PERIPHERAL CONFIGURATION DATA
      CCU     Chassis    Type     CSR    Int
    -------- ------- -------- ------ ---
1)  viop  7      0     ACM-201  0x03c0  7
2)  viop  5      1     ACM-201  0x03c8  6
3)  viop  5      0     ACM-201  0x1100  1

         *** Enter 0 for manual configuration ***

2: Ioconfig File Unit to Test [1-3,0,?]                    (1) ->
```

The applicable */ioconfig* file entries are listed (if any) above the prompt. To select a predefined controller configuration entry from the */ioconfig* file, enter the number which is found to the left of the desired entry. Entering a **0** allows each item within the controller configuration entry to be independently specified. If most, but not all, of the items associated with a given entry in */ioconfig* file are desired, select the number for that entry, back up to this prompt (via the ^ command), and specify **0** the second time. This causes the default values for the independent items to be the same as the originally selected entry.

```
3: VIOP Number [3-7,?]                                     (7) ->
```

Enter the CCU slot number for the VMEbus IOP that contains the VMEbus subsystem containing the VMEbus Async Controller.

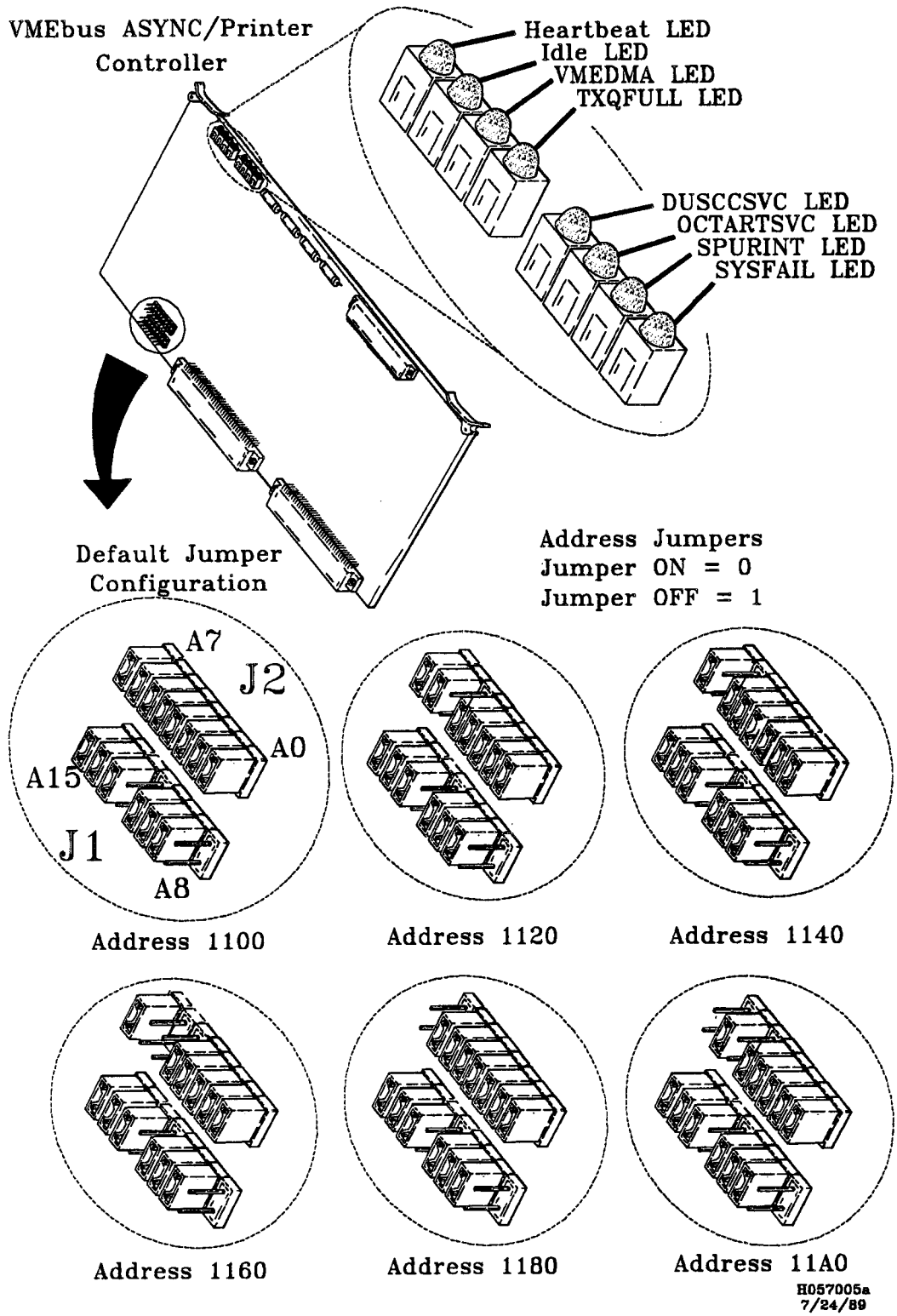
```
4: VME Chassis Number [0-1,?]                              (0) ->
```

Enter the VMEbus chassis number for the chassis where the VMEbus Async Controller is installed. If there is only 1 chassis, the number is most likely 0.

```
5: CSR of the Controller [0x10-0xffff,?]                (0x03c0) ->
```

Enter the low-order four hexadecimal digits of the VMEbus Async Controller board's base address within the VMEbus short address space. This address is controlled by jumpers on the controller. The default address is 0x03c0. The following figure shows the VMEbus Async Controller, the jumpers that control the short address space, and default jumper configuration:

Figure dev5300–5, VMEbus Async Controller Jumpers



```
6: Interrupt Number of the Controller [1-7,?]          (7) ->
```

Enter the CONVEX VMEbus interrupt number assigned to the VMEbus Async Controller board under test. This value is between 1 and 7, inclusive. The typical interrupt level is 7.

```
Baud Rate Choices:
    8000=  50       4000=  75
    2000=  110      1000=  134.5
    0800=  150      0400=  200
    0200=  300      0100=  600
    0080=  1050     0040=  1200*
    0020=  2000     0010=  2400*
    0008=  4800     0004=  9600*
    0002=  19200*   0001=  38400*
7: Select Baud Rates Mask (* indicates default) [0x0-0xffff,?]
                                                    (0x57) ->
```

This prompt allows specification of the baud rate at which the serial devices are tested. Default baud rates are marked by a asterisk (*).

> **NOTE**
>
> Selection of the options is achieved by entering the hexadecimal mask obtained by ORing the desired options (hexadecimal numbers to the left of the baud rate) together. For example, if the first two baud rates are desired (50 and 75), OR their hexadecimal masks (4000 and 8000) together and enter C000.

```
8: Port Test Mask (hex), bit 2^n for port n [0x0-0xffff,?]
                                                  (0xffff) ->
```

This prompt allows selection of which ports to test.

> **NOTE**
>
> The external loopback tests require that ports be tested in adjacent pairs, i.e., in order to test port 1, port 0 must be enabled as well. The internal loopback tests do not require any such restriction, a single port may be tested.

```
9: Enable Debug Monitor [y,n,?]                        (n) ->
```

This option allows automatic entry to the interactive debugger any time an error is detected within a subtest. The debugger may also be invoked by specifying the **-d** option at test invocation time (i.e., **dev5300[x] -d**).

```
10: Use Defaults for Remaining Parameters [y,n,?]      (y) ->
```

Answering yes in response to this prompt results in the selection of the default value for all remaining prompts. This avoids having to explicitly enter a RETURN in response to all remaining prompts.

```
** Printer On/Off Enable/Disable Options (bit mapped) **
  0x0001: Enable printer ON string before error
  0x0002: Enable printer OFF string after error

11: Select Printer On/Off Mode [0x0-0x3,?]                (0x0) ->
```

This option provides the ability to send a specified character string to the display before or after an error and its data have been displayed. Although any string up to 64 characters may be sent, the intended use is to allow the ability to selectively turn a printer on before an error is displayed and turn a printer off after an error is displayed. This is a paper saving feature when running the test over and over for several hours. Errors are only printed when both the on and off strings are enabled. This assumes a printer is connected to the auxiliary port on the display terminal where the test is running and that the auxiliary port can be turned on and off via an escape character sequence.

```
12: Enable External Loopback Tests [y,n,?]                (n) ->
```

This enables external loopback tests for the Universal Asynchronous Receiver Transmitter (UART) and Dual Universal Serial Communication Control (DUSCC) ports to be disabled. If these subtests are enabled, be sure that loopback cables (Systech loopback cable 603-030012-200) are installed in all ports specified for testing.

```
13: Ignore Errors [y,n,?]                                 (n) ->
```

This option causes the diagnostic to log errors but to continue running. Upon completion of a test the error log is printed out (if any errors occurred) but the test will be treated as though it passed. However, a cache controller error, cable error, or bus error on the VIOP will not be put in the error log and will cause the test to fail.

```
14: Select Download File [<filepath>,?]          (dev5300.xx0) ->
```

The download file is the file that is downloaded to the controller for class 2 and class 3 tests. Subtest 200 will download any *b.out* file to the controller but it should be noted that the remaining tests depend upon the proper program being executed on the VMEbus Async Controller.

```
    Printer Type Choices:
        Data Products - 0
        Centronics    - 1
15: Select Printer Type [0x0-0x1,?]                      (0x1) ->
```

The VMEbus Async Controller supports two types of printer interfaces. A **1** selects the Centronics printer interface and a **0** selects the Data Products printer interface.

```
16: Select Pattern File for Printer Test [<filepath>,?]
                                                  (dev5300.pat) ->
```

This is the file used by the printer test for the test pattern. The file can be up to 4 Kbytes in size and should not contain carriage returns.

```
17: Select Number of Characters per Line [1-132,?]        (80) ->
```

This prompt specifies the number of characters to print per line.

```
18: Add <LF> after Line [y,n,?]                    (y) ->
```

This prompt specifies whether a line feed is added after each line.

```
19: Add <CR> at end of Line [y,n,?]                (y) ->
```

This prompt specifies whether a carriage return is added at end of line.

```
20: Select number of Lines per Page [1-60,?]       (60) ->
```

This prompt asks for the number lines to print per page. After the specified number of lines are printed a form feed is issued to the printer.

```
21: Select Number of Lines to Print [1-1000,?]     (61) ->
```

This prompt specifies the total number of lines to print in the test.

```
22: Enter OK, or :NN to return to question NN [OK]  (OK) ->
```

If **OK** is entered, the test parameter menu terminates and all inputs are no longer changeable. To return to any previous prompt, enter the prompt number instead of **OK**.

VMEbus Async EPROM Self-tests

The VMEbus Async TTY/Printer Controller EPROM contains self-diagnostic routines that are executed immediately after any reset to the board or anytime power is applied. The controller EPROM is copied into instruction RAM in addresses 0x0–0x7fff. The self-tests perform initialization upon reset, downloading of Operating System driver modules, execution of self-tests, and a debug monitor (accessed from an available TTY port of the controller).

Upon reset or power up, the EPROM first disables interrupts, turns off the VMEbus DMA and the printer interface, enables bus timeouts, clears all pending interrupts, and then computes an EPROM check sum. If the check sum computation fails, a 0x55 is displayed on the controller LEDs and the processor stops. If the check sum is correct, the EPROM clears instruction RAM and then examines its VMEbus address as read from the jumpers (see Figure dev5300-5, VMEbus Async Controller Jumpers). If the controller address is 0x11c0 (see Figure dev5300-6, Jumper Setting for Debug Monitor), the controller enters the Debug Monitor, described in the "Debug Monitor" section of this test description. If the address is not 0x11c0, the EPROM starts execution of the self-tests. These self-tests are described in more detail in the following section.

Upon failure of a self-test, the self-test number is placed in the LED Display Register and displayed on the controller LEDs and the processor stops. If the controller is idle, the controller LEDs cycle. The LEDs are numbered zero through seven from left to right, respectively. The least significant bit is LED zero and the most significant bit is LED seven.

If all self-tests pass, the EPROM enables interrupt A and interrupt B, clears the SYS_FAIL bit in the Reset Register, and then waits for an interrupt.

EPROM Self-Test Descriptions

The following sections describe each VMEbus Async TTY/Printer Controller EPROM self-test.

Self-Test 1, Instruction Memory Self-Test

Each byte of the instruction RAM (address 0x0–0x3ffff) is accessed and unique data is written. The memory is then read and verified. The pattern '0xaaaaaaaa/0x55555555' is written and verified throughout memory. The pattern is then inverted and the algorithm repeated.

Self-Test 2, Memory Address Self-Test

This self-test quickly verifies longword accessibility in dual port RAM (address 0x40000000–0x4003ffff). A one is walked across the address and unique data is written and verified in dual port RAM.

Self-Test 3, DPR Memory Self-Test

Each byte of dual port RAM (address 0x40000000–0x4003ffff) is accessed and unique data is written. The memory is then read and verified. Next, the pattern '0xaaaaaaaa/0x55555555' is written and verified throughout memory. The pattern is then inverted and the algorithm repeated.

Self-Test 4, Array Register Self-Test

A walking ones/zeros test is performed on all valid bits on all read/write registers on the board. The registers tested are:

- intr #0 priority
- intr #1 priority
- intr #2 priority
- intr #3 priority
- intr #4 priority
- intr #5 priority
- intr #6 priority
- intr #7 priority
- intr #8 priority
- intr #9 priority
- intr #10 priority
- intr #11 priority
- intr #12 priority
- intr #13 priority
- intr #14 priority
- intr #15 priority
- intr #16 priority
- intr #17 priority
- intr #18 priority
- intr #19 priority
- intr #20 priority
- intr #21 priority
- intr #22 priority
- intr #23 priority
- intr #24 priority
- intr #25 priority
- intr #26 priority
- intr #27 priority
- intr #28 priority
- intr #29 priority
- intr #30 priority
- IER msb
- IER lsb
- FIR msb
- FIR lsb
- timer a base count
- timer a contol reg
- timer b base count
- timer b control reg
- vmebus map reg (msg)
- vmebus map reg (lsb)
- timeout reg
- supervisory base addr
- vmebus intr cntl reg
- vme dma addr modifier
- vme dma base addr reg msb
- vme dma base addr reg lsb
- vme dma local bar msb
- vme dma local bar lsb
- vme dma byte count
- vme dma throttle reg
- io dma 0 addr reg msb
- io dma 0 addr reg lsb
- io dma 0 byte count
- io dma 1 addr reg msb
- io dma 1 addr reg msb
- io dma 1 byte count
- io dma 2 addr reg msb
- io dma 1 byte count
- io dma 2 addr reg lsb
- io dma 3 addr reg msb
- io dma 3 addr reg lsb
- io dma 3 byte count
- DSR

Self-Test 5, Interrupt Arbitration Self-Test

The interrupt arbitration self-test verifies the ability of the board to schedule multiple simultaneous interrupts of the same priority. The self-test causes two interrupts of each priority to be requested simultaneously using the Force Interrupt Register (FIR). The self-test verifies that these interrupts are scheduled, according to priority, in a round-robin manner. Interrupt levels zero through seven are verified.

Self-Test 6, First Interrupt Self-Test

The first interrupt self-test (self-test 6) sets up the interrupt priority registers, the Interrupt Vector Base Register, and the Interrupt Enable Register (IER). The self-test enables all interrupts in the IER then causes each interrupt using the Force Interrupt Register (FIR). Each interrupt is caused twice successively and verified in the Interrupt Status Register (ISR).

Self-Test 7, Second Interrupt Self-Test

The second interrupt self-test (self-test 7) enables all possible 32 interrupts by writing the appropriate bit in the FIR. The interrupt vector, which is generated, is written to memory and verified.

Self-Test 8, Timer Self-Test

The functionality of the Timer Control Register for the two timer circuits are verified. All modes of the timers and the proper generation of interrupts are also verified for both timers.

Self-Test 9, Timer Counter Self-Test

The timer counter Self-Test walks a one across the Timer Base Count Register to verify the ability of the Present Count Register to properly decrement the timer count value.

Self-Test 10, Timer Scale Self-Test

The timer pre-scaler (value that the reference clock is divided by) functionality is verified by counting the number of iterations of a timing loop with scale set at divide by one (this is used as a reference count). The count used in the scale of one is multiplied by the inverse of the scale factor (i.e., if the scale is ½ the count is multiplied by 2, if the scale ¼ the count is multiplied by 4). The number of iterations of the timing loop with the adjusted count and scale is compared to the base count obtained with the initial scale.

Self-Test 11, Printer FIFO Self-Test

The printer FIFO is a 1-Kbyte FIFO 8 bits wide. The FIFO is filled and then read — verifying the functionality of the FIFO full and FIFO empty status bits, as well as the data integrity. The FIFO empty printer interrupt is also verified.

Self-Test 12, DUSCC Self-Test

The Dual Universal Serial Communication Controls (DUSCCs) are looped back internally and characters written to each transmit register. The self-test verifies that the characters are received as expected in the receive buffer and that the appropriate status is generated. This self-test only tests at the 9,600 baud rate, 8 bits per character with even parity.

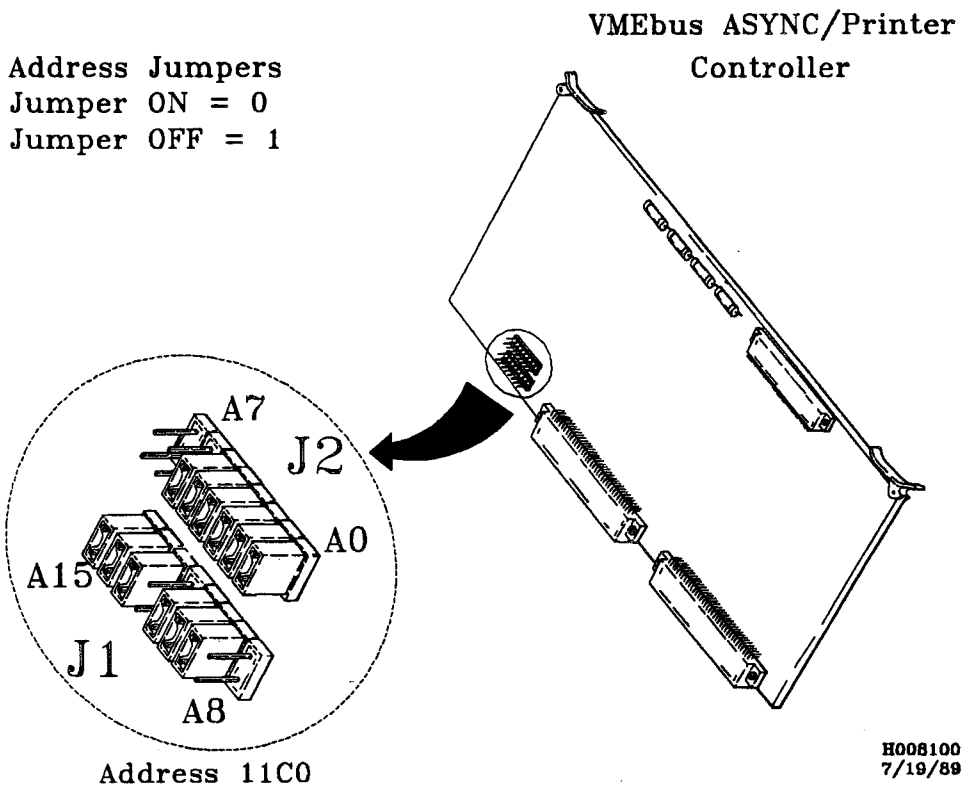
Self-Test 13, Octal UART Self-Test

The Octal UARTs are looped back internally and characters written to each transmit register. The self-test verifies that the characters are received as expected in the receive buffer and that the appropriate status is generated. This self-test only tests at the 9,600 baud rate, 8 bits per character with even parity.

Debug Monitor

The Debug Monitor within the EPROM self-test portion of this diagnostic is designed for use primarily associated with board level debugging. Using the Debug Monitor allows the VIOP and the Service Processor to be bypassed using TTY ports on the VMEbus Async Controller for board level debugging. The console must be attached to a TTY port on the VMEbus Async Controller, the controller address must be set to 0x11c0 (see the following figure), and the VMEbus chassis must be reset to invoke the Debug Monitor.

Figure dev5300–6, Jumper Settings for Debug Monitor



Upon first entering the debug monitor, the EPROM initializes the DUSCC and UART devices for 9,600 baud, 8 bits per character, 1 stop bit, and no parity. The debugger then checks each port looking for a carriage return (RETURN) at one of the TTY ports. As soon as a carriage return (RETURN) is received, that port address is used for all TTY communication until the controller is reset.

Debug Monitor Commands

The following screen shows all Debug Monitor commands. All numbers are hexadecimal.

Figure dev5300–7, Debug Monitor Commands

```
d [-bwl] a1 [a2]           - display/modify contents of locations a1 - a2
f [-bwl] a1 [a2] pattern   - fill locations a1 - a2 with pattern
s [-bwl] a1 a2 pattern     - search locations a1 - a2 for pattern
c [-bwl] a1 a2 a3          - copy block of memory a1 - a2 to address a3
r [number [number]]        - run one or more self-tests
p [-acd] [-rlt<number>]    - print test sequence to printer; -a: add <CR>,
  -c: centronics, -d: data - -r: chars/line, -l: lines/page, -t: total chars
q (if in dump/modify mode) - quit dumping/modifying
h                          - display command summary
?                          - display command summary
```

d

Usage: **d** [-bwl] **a1** [a2]

Displays and/or modifies contents of locations a1–a2 where:

-b is for byte access

-w is for word (2 bytes) access

-l is for longword (4 bytes) access (default)

If the ending address (a2) is omitted, this command enters an interactive mode that allows modification of memory. The following list gives all valid responses, while in interactive mode:

[<value>]	write optional <value> to current address; stay at thisaddress
.	stay at the present address (re-read)
-	back up to the previous address
RETURN	advance to the next address
q	write optional <value> to current address; exit interactive mode.

f

Usage: **f** [-bwl] **a1** [a2] *pattern*

Fills locations a1–a2 with *pattern*. If the ending address (a2) is omitted, only the first address (a1) is written. The options are:

-b is for byte access

-w is for word (2 bytes) access

-l is for longword (4 bytes) access (default)

s

Usage: **s** [-bwl] **a1 a2** *pattern*

Searches locations a1–a2 for *pattern*. Each time the *pattern* is matched, the address and data are displayed. The available options are:

-b is for byte access

-w is for word (2 bytes) access

-l is for longword (4 bytes) access (default)

c

Usage: **c** [-bwl] **a1 a2 a3**

Copy a block of memory from a1 to a2 to address a3 where:

-b is for byte access

-w is for word (2 bytes) access

-l is for longword (4 bytes) access (default)

r

Usage: **r** [number [number]]

Runs one or more self-tests. If **r** is entered with no arguments, the test list is displayed. Any number of tests may be specified in any order (separated by a space) but the input line may not be more than 80 characters long.

p

Usage: **p** [-acd] [-rlt<number>]

Prints test sequence to printer. The test sequence is all printable characters from 0x21 to 0x7e, repeated as needed. A line feed (0x0a) is inserted at the end of each line. A carriage return (0x0d) is then inserted if the -a option was invoked. A form feed (0x0e) is inserted after the specified number of lines have been printed. The available options are:

-a add carriage return (0x0d)

-c Centronics printer (default)

-d Data Products

-r number of characters per line (default is 80)

-l number of lines per page (default is 60)

-t total

h or ?

Usage: **h** or: Usage: **?**

Displays command summary.

Class Descriptions

The *dev5300* test contains the three classes of subtests listed in the following table:

Table dev5300–3, *dev5300* Test Classes

CLASS	DESCRIPTION
1	Basic Controller Tests
2	Download and Execute Firmware on the Controller
3	Printer FIFO and Interface Tests

All subtests contained in *dev5300* are loopable under the *dshell*.

Class 1 Subtests

Class 1 subtests consist of basic controller tests involving EPROM, parity, interrupt, and RAM. They test the controller without downloading any code to be executed on the controller. This class of subtests verifies the ability of the VIOP to access the controller, the functionality of the controller map registers, and communicates with the controller EPROM code to run each of the self-tests individually.

Table dev5300–4, Class 1 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
100	VMEbus Async Access Controller Test	00:01
101	VMEbus Async Supervisor Registers Test	00:01
102	VMEbus Async Local Map Registers Test	00:01
103	VMEbus Async VMEbus Address Match Test	00:01
104	VMEbus Async Instruction Memory Self-Test	00:13
105	VMEbus Async Memory Address Self-Test	00:08
106	VMEbus Async DPR Memory Self-Test	00:13
107	VMEbus Async Array Register Self-Test	00:08
108	VMEbus Async Interrupt Self-Test	00:08
109	VMEbus Async Interrupt Self-Test	00:08
110	VMEbus Async Interrupt Self-Test	00:08
111	VMEbus Async Timer Self-Test	00:08
112	VMEbus Async Timer Counter Self-Test	00:08
113	VMEbus Async Timer Scale Self-Test	00:08
114	VMEbus Async Printer FIFO Self-Test	00:08
115	VMEbus Async DUSCC Self-Test	00:08
116	VMEbus Async Octal UART Self-Test	00:08

Subtest 100, VMEbus Async Access Controller Test

This subtest attempts to read the controller reset register at the address specified by the user-selected entry in the *ioconfig* file or the user-specified address/VMEbus.

Subtest 101, VMEbus Async Supervisor Registers Test

This subtest will walk a one then a zero across all valid bits in all registers (which do not cause interrupts or a reset to occur) of the controller in the short address space of the VIOP. These registers and their addresses are:

- MSB of reset register (csr + 1)
- LSB of reset register (csr + 3)
- MSB of local map register (csr + 5)
- MID of local map register (csr + 7)
- LSB of local map register (csr + 9)
- MSB of VMEbus address match register (csr + 11)
- MID of VMEbus address match register (csr + 13)
- LSB of VMEbus address match register (csr + 15)
- VMEbus address modifier match register (csr + 17)

The subtest verifies register independence as well as the integrity of each register.

Subtest 102, VMEbus Async Local Map Registers Test

This subtest verifies the functionality of the map registers. A one is walked across the local map registers with mapping enabled and unique data is written and read to each valid address generated in this manner. After all valid addresses have been written in this method, all of the above addresses are generated again and the data is read back to verify access independence.

Subtest 103, VMEbus Async Address Match Test

This subtest verifies the functionality of the VMEbus address match registers. Data is written, after setting up the map registers, to a location in DPR. A one is walked across the address match registers with mapping enabled and the ability to read the data at each new valid VMEbus address generated by the walking one is verified.

Subtest 104, VMEbus Async Instruction Memory Self-Test

Each byte of the instruction RAM (address 0x0–0x3ffff) is accessed and unique data is written. The memory is then read and verified. Next, the memory has a pattern (0xaaaaaaaa/0x55555555) written and verified throughout memory. The pattern is then inverted and the algorithm repeated.

Subtest 105 VMEbus Async Memory Address Self-Test

This test is a quick verification of longword accessibility in DPR (address 0x40000000–0x4003ffff). A one is walked across the address and unique data is written and verified in DPR.

Subtest 106, VMEbus Async DPR Memory Self-Test

Each byte of DPR (address 0x40000000–0x4003ffff) is accessed and unique data is written. The memory is then read and verified. Next the memory has a pattern (0xaaaaaaaa/0x55555555) written and verified throughout memory. The pattern is then inverted and the algorithm repeated.

Subtest 107, VMEbus Async Array Register Self-Test

A walking ones/zeros test is performed on all valid bits of all read/write registers on the board. The registers to be tested are:

- intr #0 priority
- intr #1 priority
- intr #2 priority
- intr #3 priority
- intr #4 priority
- intr #5 priority
- intr #6 priority
- intr #7 priority
- intr #8 priority
- intr #9 priority
- intr #10 priority
- intr #11 priority
- intr #12 priority
- intr #13 priority
- intr #14 priority
- intr #15 priority
- intr #16 priority
- intr #17 priority
- intr #18 priority
- intr #19 priority
- intr #20 priority
- intr #21 priority
- intr #22 priority
- intr #23 priority
- intr #24 priority
- intr #25 priority
- intr #26 priority
- intr #27 priority
- intr #28 priority
- intr #29 priority
- intr #30 priority
- IER msb
- IER lsb
- FIR msb
- FIR lsb
- timer a base count
- timer a contol reg
- timer b base count
- timer b control reg
- vmebus map reg (msg)
- vmebus map reg (lsb)
- timeout reg
- supervisory base addr
- vmebus intr cntl reg
- vme dma addr modifier
- vme dma base addr reg msb
- vme dma base addr reg lsb
- vme dma local bar msb
- vme dma local bar lsb
- vme dma byte count
- vme dma throttle reg
- io dma 0 addr reg msb
- io dma 0 addr reg lsb
- io dma 0 byte count
- io dma 1 addr reg msb
- io dma 1 addr reg msb
- io dma 1 byte count
- io dma 2 addr reg msb
- io dma 1 byte count
- io dma 2 addr reg lsb
- io dma 3 addr reg msb
- io dma 3 addr reg lsb
- io dma 3 byte count
- DSR

Subtest 108, VMEbus Async Interrupt Self-Test

The interrupt arbitration subtest verifies the ability of the board to schedule multiple simultaneous interrupts of the same priority. The subtest causes two interrupts of each priority to be requested simultaneously using the Force Interrupt Register (FIR). The subtest verifies that these interrupts are scheduled, according to priority, in a round-robin manner for interrupt levels zero through seven.

Subtest 109, VMEbus Async Interrupt Self-Test

Subtest 109 sets up the interrupt priority registers, the Interrupt Vector Base Register, and the Interrupt Enable Register (IER). The subtest enables all interrupts in the IER then causes each interrupt using the Force Interrupt Register (FIR). Each interrupt is caused twice successively and verified in the Interrupt Status Register (ISR).

Subtest 110, VMEbus Async Interrupt Self-Test

Subtest 110 enables all possible 32 interrupts in the Interrupt Enable Register (IER) that are then caused by writing the appropriate bit in the FIR. The interrupt vector that is generated is written to memory to be verified.

Subtest 111, VMEbus Async Timer Self-Test

The functionality of the Timer Control Register for the two timer circuits is verified. All modes of the timers and the proper generation of interrupts are also verified for both timers.

Subtest 112, VMEbus Async Timer Counter Self-Test

A one is walked across the Timer Base Count Register. Also, the ability of the Present Count Register to properly decrement the timer count value is verified.

Subtest 113, VMEbus Async Timer Scale Self-Test

Subtest 113 verifies the timer's pre-scaler functionality by counting the number of iterations of a timing loop with scale set at divide by one (this is used as a reference count.) The count used in the scale of one is multiplied by the inverse of the scale factor (i.e., if the scale is ½ the count is multiplied by 2, if the scale ¼ the count is multiplied by four). The number of iterations of the timing loop with the adjusted count and scale is compared to the base count obtained with the initial scale.

Subtest 114, VMEbus Async Printer FIFO Self-Test

The printer FIFO (1-Kbyte FIFO, 8 bits wide) is filled and then read. The functionality of the FIFO full and FIFO empty status bits, as well as the data integrity is verified. The FIFO empty printer interrupt is also verified.

Subtest 115, VMEbus Async DUSCC Self-Test

The DUSCCs are looped back internally and characters are written to each transmit register. The subtest verifies that the characters are received as expected in the receive buffer and that the appropriate status is generated. This subtest only tests at the 9,600 baud rate, 8 bits per character with even parity.

Subtest 116, VMEbus Async Octal UART Self-Test

The octal UARTs are looped back internally and characters are written to each transmit register. The subtest verifies that the characters are received as expected in the receive buffer and that the appropriate status is generated. This subtest only tests at the 9,600 baud rate, 8 bits per character with even parity.

Class 2 Subtests

The class 2 subtests first download a firmware module to execute on the controller. This class of tests then communicates with the downloaded module on the controller to perform the following tests:

Table dev5300–5, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	VMEbus Async Download Test	00:04
201	VMEbus Async Access Test	00:02
202	VMEbus Async Interrupt Test	00:02
203	VMEbus Async Errors Test	00:02
204	VMEbus Async Basic DMA Test	01:24
205	VMEbus Async DMA Counter Test	00:02
206	VMEbus Async DMA Suspend Test	00:02
207	VMEbus Async DMA Throttle Test	00:02
208	VMEbus Async DMA Error Test	00:02
209	VMEbus Async Octal UART Internal Loopback Test	13:20
210	VMEbus Async DUSCC Internal Loopback Test	12:50
211	VMEbus Async Octal UART External Loopback Test	13:20
212	VMEbus Async DUSCC External Loopback Test	12:50

Subtest 200, VMEbus Async Download Test

This subtest verifies the ability to execute a downloaded module in the controller. The code to be executed on the controller is written into the instruction RAM via the map registers, then read back to verify the download. The controller is then reset with the EPROM mapped out. The downloaded code (which starts at address 0) then begins execution. The clearing of the

"SYSFAIL" bit in the controller reset register indicates a successful boot.

Subtest 201 VMEbus Async Access Test

This subtest verifies that the 68020 on the controller has the ability to perform VMEbus accesses to and from a VIOP window register. The subtest verifies reads and writes of 1 byte to 11 bytes to addresses with offsets of 0 byte to 3 bytes.

Subtest 202, VMEbus Async Interrupt Test

This subtest verifies the ability of the controller to properly generate VMEbus interrupts as well as receive interrupts. The controller interrupt, acknowledge interrupt, is also verified. The subtest verifies the ability of the controller to recognize the "mailbox" interrupts. The VIOP generates these interrupts by writing a specific bit in the reset register of the controller. The ability of the controller to take these one at a time as well as simultaneously is verified.

Subtest 203, VMEbus Async Errors Test

This subtest verifies the ability of the controller to recognize the various bus timeout conditions. There are three types of timeouts: VMEbus arbitration, VMEbus dtack, and local bus. The subtest verifies that the board signals bus error for all required conditions as well as verifying that the bus error source register is correct and the bus error exception routine is properly invoked.

Subtest 204, VMEbus Async Basic DMA Test

This subtest verifies the ability of the controller to perform DMA accesses to and from the VIOP. This subtest verifies normal DMA operation of reads and writes of transfers of 1 bytes to 12 bytes at addresses with offsets of 0 byte to 3 bytes.

Subtest 205, VMEbus Async DMA Counter Test

This subtest verifies the counting logic of the VMEbus DMA Controller counter. A one is walked across the DMA counter register and the DMA transfer is started. The transfer is then stopped and the Present Count Register is examined to verify that the count has decremented properly.

Subtest 206, VMEbus Async DMA Suspend Test

This subtest verifies that the DMA Controller suspends a DMA transfer upon assertion of the suspend bit. A transfer is started then suspended. After waiting, the Current Byte Count Register is examined to verify that the transfer was suspended.

Subtest 207, VMEbus Async DMA Throttle Test

This subtest validates the ability of the controller to throttle DMA operations by setting the Throttle Register to four. The DMA transfer is then started normally. After starting the DMA transfer, the 68020 immediately attempts to read the VMEbus address of the starting DMA

transfer address plus four times the transfer size. The DMA gives up the bus after four accesses and the 68020 is able to complete its read. Since this memory was previously cleared the 68020 reads a zero. Successive reads to this address results in the DMA (non zero) data being read.

Subtest 208 VMEbus Async DMA Error Test

This subtest verifies the ability of the DMA Controller to recognize error conditions and respond to them properly. All conditions causing a configuration error, a count error, a bus arbitration error, and a bus error are tested.

Subtest 209, VMEbus Async Octal UART Internal Loopback Test

This subtest verifies the functionality of the octal UART in local loopback mode. The subtest uses all baud rates supported by the devices, only one stop bit per character. Both 7-bit and 8-bit characters are used with even, odd, and no parity generated for each character. The baud rates tested are selectable in the test parameter menu that is presented after test invocation. Since synchronous communication requires panel changes (which is not currently supported) only asynchronous communication is tested.

Subtest 210, VMEbus Async DUSCC Internal Loopback Test

This subtest verifies the functionality of the DUSCC devices in local loopback mode. The subtest uses all baud rates supported by the devices, only one stop bit per character. Both 7-bit and 8-bit characters are used with even, odd, and no parity generated for each character. The baud rates tested are selectable in the test parameter menu that is presented after test invocation. Since synchronous communication requires panel changes (which is not currently supported) only asynchronous communication is tested.

Subtest 211, VMEbus Async Octal UART External Loopback Test

This subtest verifies the octal UART device with loopback cables attached. This subtest uses the same algorithm as Subtest 210. Again, only asynchronous communication is tested. Data Terminal Ready (DTR) and Data Send Ready (DSR) loopback are tested in this subtest as well.

Subtest 212, VMEbus Async DUSCC External Loopback Test

This subtest verifies the DUSCC devices with loopback cables attached. This subtest uses the same algorithm as the Subtest 210. Again, only asynchronous communication is tested. Data Terminal Ready (DTR) and Data Send Ready (DSR) loopback are tested in this subtest as well.

Class 3 Subtest

The purpose of the class 3 test is to test the printer FIFO and interface. The same module that is downloaded for the class 2 tests is also downloaded for this test. Subtest 300 is the only test in this class, as indicated in the following table:

Table dev5300–6, Class 3 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
300	VMEbus Async Printer Test	00:16

Subtest 300, VMEbus Async Printer Test

This subtest verifies the printer subsystem. In order to properly complete this subtest, a printer must be attached to the console. The subtest allows the specification of a file containing the pattern to print, the number of characters per line, the number of lines per page, and the number of pages to print. If the printer is not entered in the ioconfig file, a warning is printed to the terminal and the subtest is not executed.

Interactive Debugger

The diagnostic provides an interactive debugger that supports the ability to execute commands from a script file. This allows more debug flexibility. Invocation of the interactive debugger is achieved by using the **-d** option when invoking the diagnostic (enter **dev5300**[x] **-d**). Also, the interactive debugger can be invoked by entering **y** to the "Enable Debug Monitor?" prompt. No subtests are executed and the debugger is invoked.

Once the interactive debugger is invoked, online help commands are available. By entering **help** (RETURN), the following screen is displayed:

Figure dev5300–8, Interactive Debugger Online Help

```
Input base specification:
    0dNN - decimal,  0xNN or NN - hexadecimal,  the default is hexadecimal

Meta-command sequences:
   ![UNIX_CMD]       - execute UNIX_CMD
   !![UNIX_CMD]      - fork a shell and execute UNIX_CMD (allows redirection)
   <FILE             - redirect input from FILE (recursive)
   <<FILE            - end input from current file and change input to FILE

Commands:
    Commands may be abbreviated as long as the abbreviation is unique.

    help    [COMMAND ...]                    - display general or specific help
    cd      [DIRECTORY]                      - change to DIRECTORY
    quit                                     - exit debug mode
    pause   [-n] [seconds]                   - pause for <C/R> or seconds
    mb      begin [end] [step]               - modify/[dump] bytes on CCU
    mw      begin [end] [step]               - modify/[dump] words on CCU
    ml      begin [end] [step]               - modify/[dump] longs on CCU
    mmb     begin [end] [step]               - modify/[dump] bytes in MM
    mmw     begin [end] [step]               - modify/[dump] words in MM
    mml     begin [end] [step]               - modify/[dump] longs in MM
    fb      begin [end] value [incr [step]] - fill bytes on CCU
    fw      begin [end] value [incr [step]] - fill words on CCU
    fl      begin [end] value [incr [step]] - fill longs on CCU
    reset   [0,1]                            - reset Vasync controller
    map     vme local                        - map vme address to Vasync
    load    file                             - download file to Vasync
    csrreg                                   - dump controller's VME regs
    vdma                                     - dump controller's VME DMA regs
    iodma    [0-3]                           - dump controller's I/O DMA regs
```

In addition to the help screen in the previous figure, help for each specific command is obtained by entering:

help *command*

In the previous sequence, replace *command* with the desired debugger command. Abbreviations of the desired commands may be used. For example, for help with all commands that start with the letter "r," enter:

help r

Interactive Debugger Command Descriptions

help

Usage: **help** [COMMAND ...]

Displays general or specific help, where COMMAND is replaced with the desired interactive debugger command. Specific help is displayed for COMMAND. The COMMAND may be an abbreviation. The following example would list help for all commands that start with the letter "r":

help r

cd

Usage: **cd** [PATH]

Changes to desired directory, where PATH may be any valid directory path. If PATH is omitted, the default path is $HOME or / if $HOME not set.

pause

Usage: **pause** [-n] [seconds]

Wait for specified amount of time or for a RETURN if the time is omitted, where:

-n means do not echo the pause message

seconds specifies the number of seconds to pause

mb, mw, ml

Usage: **mb begin** [end] [step]
mw begin [end] [step]
ml begin [end] [step]

Displays or modifies, or both, CCU address space in byte-at-a-time mode (mb), word-at-a-time mode (mw), or long-word-at-a-time mode (ml), where:

- **begin** is the initial address
- **end** is the ending address (optional)
- **step** is the address increment (optional (default is access size))

If the ending address is omitted, this command enters an interactive mode that allows modification of memory. The following list gives the valid responses while in interactive mode:

[<value>]	write optional <value> to current address, advance to next address
[<value>]=	write optional <value> to current address, and stay at the present address (re-read)
[<value>]^[N]	write optional <value> to current address, move to address N (address 0 if N is omitted)
[<value>]+[N]	write optional <value> to current address, advance to the next address (N addresses if N is specified)

[<value>]-[N]	write optional <value> to current address, back up to the previous address (N addresses if N is specified)
[<value>]q	write optional <value> to current address, exit interactive mode

Multiple commands may be specified on the same line. A comma or space may be used to separate the commands or value as shown in the following example:

```
Debug mode -> mb c03fc1
<CCU:c03fc1> = 1c 00=ff,1q
```

Where: **1c 00=ff,1q** is an example of executing multiple commands on the same line. This sequence modifies the byte at address 0xc03fc1 to 0, re-reads and displays the new value, modifies the byte to 0xff, skips to address 0xc03fc2 and modifies it to a 0x1, and then quits interactive mode.

mmb, mmw, mml

Usage: **mmb begin** [end] [step]
mmw begin [end] [step]
mml begin [end] [step]

Displays or modifies (or both) main memory address space in byte-at-a-time mode (mmb), word-at-a-time mode (mmw), or long-word-at-a-time mode (mml), where:

- **begin** is the initial address
- **end** is the ending address (optional)
- **step** is the address increment (optional (default is access size))

If the ending address is omitted, this command enters an interactive mode that allows modification of memory. The following list gives all valid responses while in interactive mode:

[<value>]	write optional <value> to current address, advance to next address
[<value>]=	write optional <value> to current address, and stay at the present address (re-read)
[<value>]^[N]	write optional <value> to current address, move to address N (address 0 if N is omitted)
[<value>]+[N]	write optional <value> to current address, advance to the next address (N addresses if N is specified)
[<value>]-[N]	write optional <value> to current address, back up to the previous address (N addresses if N is specified)
[<value>]q	write optional <value> to current address, exit interactive mode

Multiple commands may be specified on the same line. A comma or space may be used to separate the commands or values as shown in the following example:

```
Debug mode -> mmb c03fc1
<Main-Mem:c03fc1> = 1c 00=ff,1q
```

Where: **1c 00=ff,1q** is an example of executing multiple commands on the same line. This sequence modifies the byte at main memory address 0xc03fc1 to 0, re-reads and displays the new value, modifies the byte to 0xff, skips to address 0xc03fc2 and modifies it to a 0x1, and then quits interactive mode.

fb, fw, fl

Usage: **fb begin** [end] **value** [incr [step]]
fw begin [end] **value** [incr [step]]
fl begin [end] **value** [incr [step]]

Fills memory with specified pattern in byte-at-a-time mode (fb), word-at-a-time mode (fw), or longword-at-a-time move (fl), where:

- **begin** is the starting address
- **end** is the ending address
- **value** is the initial fill value
- **incr** is the fill value increment
- **step** is the address increment

reset

Usage: **reset** [0,1]

Resets the VMEbus Async Controller by writing (ORing) a one into the Reset Register at address CSR + 1. Then releases reset by ANDing with 0xfe. If reset is issued with a 0, EPROM is mapped out. If reset is issued with a 1, EPROM is mapped in.

echo

Usage: **echo** [-n] [arg ...]

Writes arguments separated by blanks and terminated by a newline to the display, where:

-n does not echo the terminating newline character

quit

Usage: **quit**

Typing **quit** exits the interactive debugger.

map

Usage: **map vme_address local_address**

This command sets up the VMEbus Async Controller to map 4 Kbytes of its internal memory space starting at (local_address & 0xfffff000) to a vme_address. The following list shows what chassis goes with what controller and what address modifier is associated with these addresses:

Addresses 0x1000000 to 0x13fffff are chassis 0, address modifier 0x3d

Addresses 0x1400000 to 0x17fffff are chassis 1, address modifier 0x3d

Addresses 0x1800000 to 0x1bfffff are chassis 0, address modifier 0x0d

Addresses 0x1c00000 to 0x1fffffff are chassis 1, address modifier 0x0d

csrreg

Usage: **csrreg**

Dumps the registers visible in short VMEbus address space. These are the reset, the local map, VMEbus address map, and address map registers.

vdma

Usage: **vdma**

Dumps the controller VMEbus DMA registers. These are the control, status, count, local base address, VMEbus base address, throttle, and current count registers.

iodma

Usage: **iodma** [0 - 3]

Dumps the controller I/O DMA registers. These are the control, status, count, memory base address, and current count registers.

Error Messages

Two basic types of error conditions can occur when executing *dev5300*. If an error occurs during the controller EPROM self-tests (i.e., during a reset to the controller or when power is applied to the controller), no error messages are output to the console. The self-test error code is displayed on the controller LEDs and is also stored in the LED Display Register (refer to the "VMEbus Async EPROM Self-Tests" section within this test description for more information).

If an error occurs during execution of *dev5300* that is associated with the diagnostics subtests, errors are output to the console. Each error contains header information with the date and time, and the diagnostic name, class, and subtest. The following is an example of the header information:

Figure dev5300–9, Error Message Header Format

```
*****  Sun Jul 16 15:04:10 1989  *****
Test:    dev5300.t  1.1    Class: 1    Subtest: 100 1.2   Count: 1    Error: 0
Failed:  VMEbus Vasync Access Controller Test
```

Also, at the end or each error message, a footer is printed containing the diagnostics name and the elapsed time. The following is an example of a footer:

Figure dev5300–10, Error Message Footer Example

```
Test 'dev5300.t' failed
Elapsed time:   0:00:03
```

The following are the different error messages that are printed with the header and footer information:

```
Error #0x1: Invalid command
Invalid Command: 0x1

Error #0x2: VIOP Fatal Exception Error

Error #0x3: Data Miscompare
Expected: 0x0   Actual 0x1   at address 0x0

Error #0x4: VIOP Window Allocation Error

Error #0x5: VIOP Checksum Error
Expected: 0x0   Actual 0x1
Main Memory Address: 0x0  VIOP Window Address: 0x0

Error #0x6: VIOP Download Error
Read 0x0 from 0x0 in Main Memory thru 0x0
Read 0x1 from 0x0 in Vasync at mapped address 0x0

Error #0x7: Vasync Reset/Boot Error
Controller did not clear SYS_FAIL bit after reset
Expected: 0x00   Actual 0x01   in CSR + 1

Error #0x8: Vasync Controller Timeout
Controller Timed Out

Error #0x9: Vasync Device Status
Expected: 0x00   Actual 0x01   at address 0x0
```

```
Error #0x10: Vasync Timer Counter
Timer Counter Register Address: 0x0
Expected: 0x0000   Actual 0x0001

Error #0xa: Vasync Device Status
Expected: 0x0000   Actual 0x0001   at address 0x0

Error #0xb: Vasync Data Miscompare
Expected: 0x00   Actual 0x01   at address 0x0

Error #0xc: Vasync Data Miscompare
Expected: 0x0000   Actual 0x0001   at address 0x0

Error #0xd: Vasync Data Miscompare
Expected: 0x00000000   Actual 0x00000001   at address 0x0

Error #0xe: Vasync Interrupt Status
Expected Interrupt Status: 0x00000000  Actual   Interrupt Status: 0x00000001

Error #0xf: Vasync Interrupt Count
Expected Interrupt #: 0x00000000  Actual   Interrupt #: 0x00000001

Error #0x11: Invalid command
Invalid Command: 0x1

Error #0x12: Vasync Interrupt Enable
Expected IER: 0x00000000  Actual   IER: 0x00000001

Error #0x13: Vasync VME DMA Throttle
Controller failed to throttle properly
Expected: 0000
Actual  : 0001

Error #0x14: Vasync Local Bus Error
Unexpected Bus Error attempting to read address 0
Expected Bus Error: 0000
Actual Bus Error  : 0001

Unknown Error Number: 0x15
```

dev5500

VMEbus Ethernet Controller Test

Overview

The *dev5500* test is designed to verify that the Excelan EXOS/202 Ethernet controller board operates properly. The *dev5500* test verifies the VIOP-to-controller interface and triggers the controller board's built-in self-test.

Prerequisites and Required Equipment

In order to run the *dev5500* test, the following are needed:

Table dev5500–1, Hardware Requirements

C1, C120	C200 Series
EXOS/202 Controller	EXOS/202 Controller
VBCU	VBCU
VIOP	VIOP
MCU	Memory System[1]
MAU	CPX
SPU	SP2
HIA	HIA
HSP	HSP
FSE	FSE
	PIA

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

NOTE

A *delni* module must be used to run the Class 1 and Class 4 tests. The *delni* module must be connected to the board under test with a CONVEX cable 601-150001-200.

Test Invocation

The *dev5500* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev5500* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user. The prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

Figure dev5500–1, Test Invocation Sequence

```
(spu)>  cd /mnt/test RETURN
(spu)>  sysreset RETURN
(spu)>  mminit -s RETURN
(spu)>  dshell RETURN

CONVEX DIAGNOSTICS SHELL

: test dev5500 [-c [class number(s)]] [-s [subtest number(s)]] [+>filename] RETURN
```

NOTE

After entering **dshell**, specific changes may be made to the *dshell* parameters. Refer to the "Dshell Overview" chapter in this manual for more information.

Entering only **test dev5500** executes all subtests sequentially. Specific class(es) of subtest(s) or one or more individual subtests can be executed by using the **-c** or **-s** options, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter within this manual. Using the [+> *filename*] extension causes all test results to be appended to *filename* in addition to printing on the console.

The following alternate test invocation procedure may be required in some cases; however, the CPU *must* be running:

CAUTION

The user response, **initall**, is typically required if the *initall* utility has not been run since the last power up. However, if any problems have occurred subsequent to the last time *initall* was run, (i.e., system crash, hard error, or failure of previous diagnostic), it should be run again. In this case, failure to run *initall* could result in invalid test results.

NOTE

The *initall* utility requires a significant amount of time (2 to 3 minutes depending on if the control stores have been previously loaded) to execute. If no system abnormalities have occurred subsequent to the last time the system was booted or *initall* was executed, it is not necessary to run *initall*.

Figure dev5500–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> initall RETURN
(spu)> dshell RETURN
CONVEX DIAGNOSTICS SHELL
: test dev5500 [-c [class number(s)]] [-s [subtest number(s)]] [+> filename] RETURN
```

Test Parameter Menu

Once the test is invoked, test menu prompts are displayed allowing selection of default switches. The first prompt determines which test parameters are displayed. To test a device not listed in the configuration file, answer the first prompt with **0** and prompts two through nine are displayed one line at a time. Prompts two through eight allow the user to describe the location of the controller to be tested. However, answering **1** (the number representing the device to test) to the first prompt causes prompts two through fives to be skipped.

The following figure shows all prompts, with their possible answers (in brackets [ ]), and their default answers (in parenthesis ( )). The prompts and responses in the following figure appear sequentially on the screen, one line at a time. All possible prompts and responses are shown in the following figure for convenience.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev5500–2, Getting Help During Test Parameter Entry

CHARACTER	DESCRIPTION
?	Displays this help menu
h	Provides help for a specific prompt
i	Displays the Iioconfig file

After the desired help information displays, the system beeps and redisplays the last prompt.

The **Test Parameter Menu** illustrates *all* questions that can be displayed during test parameter input. However, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially. However, the numbers displayed on the screen during testing may not correspond to those shown in the example **Test Parameter Menu**, as the questions illustrated are examples only.

Figure dev5500–3, *dev5500* Test Parameter Menu

```
                    ENTER TEST PARAMETERS

    []          Encloses allowed input ranges or values
    ()          Encloses the default value
    ^           Returns to the previous prompt
    :nn         Returns to the prompt # nn
    :           Returns to the first unsatisfied prompt
    :?          Reviews previous entries


                PERIPHERAL CONFIGURATION DATA
      CCU      Chassis  Type           CSR    Int     Unit    Type
    -------    -------  ---------      -----  ---     ----    -------
1)  viop  5      0      LAN-201        0x0     0        0     ex


1: Device Selection [0,1]                          (0) ->
2: VIOP [3-7]                                      (5) ->
3: VMEbus Chassis [0-1]                            (0) ->
4: Controller Offset in VMEbus [0x0-0xffff]
                                                (0x8000) ->
5: Controller Interrupt [0-7]                      (5) ->
6: Subtest loop count [10-1000]                  (100) ->
7: Transceiver connected to active ethernet? [y,n]
                                                   (y) ->
8: Run machine <-> machine comm test? [y,n]        (n) ->
9: Enter OK, or :NN to return to question NN [OK]
                                                  (OK) ->

Device 0 = user defined configuration
```

At any time during the test parameter sequence, several options are available as denoted at the top of the Test Parameter Menu. The following list summarizes the available options:

:nn — Returns to an earlier prompt (n is the prompt number)

: — Advances to the next unanswered prompt

:? — Displays (reviews) all responses up to the current prompt

? — Request help for the current prompt (if available)

^ — Return to the previous prompt

Prompt Explanations

A description of the meaning of each prompt follows:

```
Device Selection [0,1]                    (0) ->
```

The first prompt determines which test parameters are displayed. By responding with **0** or (RETURN), prompts 2 through 8 are displayed one line at a time. These prompts allow specification and testing of a device not listed in the configuration file . Prompts 2 through 8 allow description of the location of the controller to be tested. However, if **1** (the number representing the device to test) is entered to the first prompt, prompts 2 through 4 are displayed one line at a time.

```
VIOP [3-7]                                (5) ->
```

This prompt allows selection fo the position of the VIOP in the CPU card cage with a value ranging from [**3-7**].

```
VMEbus Chassis [0-1]                      (0) ->
```

If a response of **0** or (RETURN) is entered, then VMEbus chassis 0 is selected. However, if **1** is entered, VMEbus chassis 1 is selected.

```
Controller Offset in VMEbus [0x0-0xffff]
                                      (0x8000) ->
```

If **0x8000** or (RETURN) is entered, then the test assumes this is the controller address. If the controller to be tested is not at this address then the test fails.

```
Controller Interrupt [1-7]                (5) ->
```

If a **1** or (RETURN) is entered, then interrupt one is used by the controller when an I/O operation completes to interrupt the VIOP. However, if a value in the range of [**2-7**] is entered, this interrupt is used. There is only one requirement when choosing an interrupt number, each controller in a VME chassis must have unique interrupt number. Controllers in different chassis can use the same interrupt number.

```
Subtest loop count [10-1000]            (100) ->
```

If a **100** or (RETURN) is entered, the number of subtest iterations is set to 100. However, if a value in the range of [**10-99**, **101-1000**] is entered, the number of subtest iterations is set to this value. If a value not in the range of [10-1000] is entered, the prompt is redisplayed.

```
Transceiver connected to active ethernet? [y,n]
                                          (y) ->
```

If a **y** or (RETURN) is entered, Class 2 subtests are not allowed to execute since the subtests require an inactive Ethernet for proper operation. However, if **n** is entered, then Class 2 subtests are allowed to execute.

```
Run machine <-> machine comm test? [y,n]     (n) ->
```

If **n** or (RETURN) is entered, then the Class 4 subtest is not allowed to execute. However, is **y** is entered, the Class 4 subtest is allowed to execute.

```
Enter OK, or :NN to return to question NN [OK]
                                          (OK) ->
```

If **OK** or (RETURN) is entered, the test parameter menu terminates and all inputs are no longer changeable.

After all the test parameters are entered, a test parameter summary displays the entries. If standard output is directed to a disk file, the test parameter summary is also written to the disk file.

Figure dev5500–4, Sample Test Parameter Summary

```
                TEST PARAMETER SUMMARY

Device selection                                : 0
VIOP                                            : 5
VMEbus Chassis                                  : 0
Controller Offset in VMEbus                     : 0x8000
Controller Interrupt                            : 5
Subtest loop count                              : 100
Transceiver connected to active ethernet?       : y
Run machine <-> machine comm test?              : n
Enter OK, or :NN to return to question NN       : OK
```

Hardware Initialization Sequence

After the last prompt is entered, and before test code execution, the following events occur:

- A sysreset is performed
- Main memory is allocated for the test
- SPU windows to main memory are initialized
- SPU local test variables are initialized
- The VIOP is booted and loaded
- A driver on the VIOP is started
- VIOP local test variables are initialized

After all the above events have occurred, the test code is started.

Class Descriptions

The VME Ethernet controller test *dev5500* contains four classes of subtests. The following table lists each class of subtests:

Table dev5500–3, *dev5500* Test Classes

CLASS	DESCRIPTION
1	EXOS/202 Ethernet controller access test
2	EXOS/202 Ethernet controller functional tests
3	EXOS/202 Ethernet controller online test
4	EXOS/202 Ethernet controller net transmit test

Class 1 Subtest

The EXOS/202 Ethernet controller access test verifies the basic interface from the VIOP to the controller. This ensures that the controller responds to the I/O address expected, and passes an internal self-test.

Table dev5500–4, Class 1 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
100	Controller to Host Access	0:05

Subtest 100, Controller to Host Access

Subtest 100 verifies the basic access paths. The subtest resets the controller board to verify that VIOP can access the controller, and that the controller will automatically run a self-test after reset. Next, the VIOP commands the controller to configure itself from a table in VIOP local memory. This tests the controller's ability to access VIOP local memory. Then the controller is commanded to configure itself from main memory to test controller-to-main memory access.

Class 2 Subtests

The EXOS/202 Ethernet controller functional tests verify the ability of the controller to transmit and receive various Ethernet packets. While in the *Ethernet* mode (with the use of a *delni* module connected to the board under test), these subtests transmit packets using an internal transmit with self-receive command, and transmit messages to verify the controller's address filtering. The "scatter/gather" operation of the controller is also tested by targeting data blocks to specific memory blocks.

> **NOTE**
>
> The *delni* module must be connected to the board under test with a CONVEX cable 601-150001-200.

Each Class 2 subtest resets and reconfigures the controller at the start of the subtest. This allows the subtests to be run in any order. Each subtest can loop for a user-entered number of passes.

Table dev5500–5, Class 2 Subtests

SUBTEST	DESCRIPTION	TIME (min:sec)
200	Real Physical Slot Xmit/Recv	0:20
201	Modified Physical Slot Xmit/Recv	0:20
202	Broadcast Slot Xmit/Recv	0:20
203	Real Physical/Broadcast Slot Xmit/Recv	0:40
204	Modified Physical/Broadcast Slot Xmit/Recv	0:40
205	Foreign Address Rejection Xmit/Recv	1:10
206	Scatter/Gather Operation	0:30

Subtest 200, Real Physical Slot Xmit/Recv

Subtest 200 transmits and receives packets sent to the *real* physical address of the controller. (The *real* address slot is the one that is assigned to the board by the manufacturer.)

Subtest 201, Modified Physical Slot Xmit/Recv

Subtest 201 transmits and receives packets sent to the modified physical address of the controller. This tests the controller's ability to change the address associated with a given slot, but still transmit and receive Ethernet packets.

Subtest 202, Broadcast Slot Xmit/Recv

Subtest 202 transmits and receives packets sent to the Ethernet broadcast address. Each broadcast packet is received by all controllers on the Ethernet.

Subtest 203, Real Physical/Broadcast Slot Xmit/Recv

Subtest 203 transmits and receives packets sent to the broadcast and physical address of the controller. The subtest transmits both a broadcast and a physical address packet before attempting to receive any packet. This checks the controller's ability to save packets while waiting for a receive buffer to be supplied by the host computer.

Subtest 204, Modified Physical/Broadcast Slot Xmit/Recv

Subtest 204 transmits and receives packets sent to the broadcast and modified physical address of the controller.

Subtest 205, Foreign Address Rejection Xmit/Recv

Subtest 205 transmits and receives packets sent to the broadcast and physical address of the controller. Another packet address is also sent out to verify that the controller is rejecting packets destined for other controllers.

Subtest 206, Scatter/Gather Operation

Subtest 206 tests for both transmits and receives. The address used is the controller's *real* physical address. This subtest varies the scatter/gather function from 2 blocks to 8 blocks. Each packet is transmitted and received with the same packet split.

Class 3 Subtest

The EXOS/202 Ethernet controller online test consists of subtest that can be executed on an active Ethernet. This allows the test program to execute without changing the configuration of the hardware. These subtests do not transmit or receive the "broadcast" type Ethernet packets.

Table dev5500–6, Class 3 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
300	Real Physical Slot Only Xmit/Recv	0:20

Subtest 300, Real Physical Slot Only Xmit/Recv

Subtest 300 only transmits and receives packets on the *real* physical slot. The broadcast slot is disabled. This subtest can be run on an active Ethernet without becoming confused by other packets, unless the board is not rejecting packets properly.

Class 4 Subtest

The EXOS/202 Ethernet controller online test consists of a subtest that transmit and receive packets between two machines on an Ethernet. This requires that Subtest 400 be running on the two machines used in the test. This further requires that no other machines are active on the Ethernet. The test will send a user-entered number of packets and expect to receive the same number of packets from the target machine.

> **NOTE**
>
> The *delni* module must be connected to the board under test with a CONVEX cable 601-150001-200.

Table dev5500–7, Class 4 Subtest

SUBTEST	DESCRIPTION	TIME (min:sec)
400	Machine to Machine Xmit/Recv	0:20

Subtest 400, Machine to Machine Xmit/Recv

Subtest 400 transmits and receives packets over an active Ethernet. The test uses broadcast message addresses initially to determine the address of the other target machine on the Ethernet. The test then sends a user-entered number of packets to the target machine's address and expects to receive an equal number of packets. This subtest cannot be run on an active Ethernet without confusing the other machines on the Ethernet.

Subtest Completion Messages

When the requested subtest(s) has completed, a subtest(s) completion message(s) is displayed. Sample subtest completion messages are shown in the following figure:

Figure dev5500–5, Sample Subtest Completion Messages

```
Subtest 100     0:00:02         passed
Subtest 200     0:00:19         passed
Subtest 201     0:00:19         passed
Subtest 202     0:00:19         passed
Subtest 203     0:00:37         passed
Subtest 204     0:00:37         passed
Subtest 205     0:00:02         failed
```

Subtest Error Messages

Whenever an error is detected, an appropriate error message based on the error reporting flags of the *dshell* is displayed. A sample subtest error message is shown in the following figure:

Figure dev5500–6, Sample Error Message

```
*****  Mon Feb 22 17:02:27 1988  *****
Test:    dev5500.t  1.1    Class: 1    Subtest: 100 1.2   Count: 1  Error: 0
Failed:  Controller to host access test

Cmd: access registers command, Error: Unknown error 0
```

The following error messages are for all subtests:

`Cmd: <CMD>, Error: <ERR>`

Where <CMD> is equal to one of the following strings:

- nop command to the IOP
- access registers command
- initialize in local memory
- initialize in C1 memory
- send message
- test for pending message
- receive message

And <ERR> is equal to one of the following strings:

> **NOTE**
>
> XX and YY are variables representing hexadecimal status numbers.

- unknown return code 0
- command timeout return code
- unknown command
- Reg acc fail/ self-test fail Expected Status XX, Actual Status YY
- not ready for byte 1 Expected Status XX, Actual Status YY
- not ready for byte 2 Expected Status XX, Actual Status YY
- self-test fail on configure
- accept fail on configure Expected Status XX, Actual Status YY
- configuration error
- command to controller timeout

- `host to exos buffer busy`
- `exos to host buffer busy`
- `message request code invalid`
- `xmit/recv block cnt invalid`
- `statistics block cnt invalid`

A valid message could be the following:

```
Cmd: initialize in local memory, Error: accept fail on configure
Expected Status XX, Actual Status YY
```

or

```
Cmd: send message, Error: xmit/recv block cnt invalid
```

Test End Message

An end message is displayed when the test has completed. A sample end message is shown in the following figure:

Figure dev5500–7, Sample End Message

```
Frames sent/received with no errors          1300/1200
Frames aborted with excess collisions        0
Frames transmitted with heartbeat absent     0
Frames received with alignment errors        0
Frames received with CRC errors              0
Frames lost                                  0

Test 'dev5500.t' passed
Elapsed time:   0:02:17
:
```

dev_ultra

VMEbus UltraNet Controller Test

Overview

The *dev_ultra* test is a functional test for the CONVEX VMEbus UltraNet controller. This test verifies the proper operation of the CONVEX VMEbus UltraNet controller in the CONVEX VMEbus I/O environment.

Specifically, *dev_ultra* is designed to accomplish the following:

- Verify the functional ability of the VMEbus UltraNet controller to operate in the CONVEX VMEbus I/O environment. This includes VMEbus access and interrupt generation.
- Verify that the VMEbus UltraNet controller can transmit and receive data via internal loopback paths.
- Verify that the VMEbus UltraNet controller can transmit and receive data via an external transceiver and loopback cable.

The *dev_ultra* test uses the same VMEbus I/O Processor (VIOP) code as the ConvexOS operating system. All communications with the VIOP use the same Event-Governed Operating System (EGOS) and the Message-Based System (MBS) used by the ConvexOS operating system. This means that *dev_ultra* tests the communication paths used in a normal operating environment.

Prerequisites and Required Equipment

The following table lists the required hardware depending on the type of machine under test:

Table dev_ultra–1, Hardware Requirements

C1, C120	C200 Series
MCU	Memory System[1]
MAU	CPX
SPU	SP2
VIOP	VIOP
VBCU	PIA
VMEbus UltraNet controller	VBCU
	VMEbus UltraNet controller

[1] Memory System consists of a minimum of one pair of memory boards (one odd and one even).

Subtest 201 requires a loopback cable (Part Number TBD) to execute. However, if two machines

are directly connected via VMEbus UltraNet controllers, Subtest 201 can be executed.

> **NOTE**
>
> Refer to the description of Subtest 201 for the procedure required to execute Subtest 201 in the direct connection mode without loopback cables.

Test Invocation

The *dev_ultra* test executes under the Diagnostic Shell (*dshell*) and supports all the features of the *dshell*. The *dshell* permits tests to be initiated in any order.

To invoke the *dev_ultra* test, use the procedure shown in the following figure. All responses in **boldface** are entered by the user.

> **NOTE**
>
> Use following test invocation sequence for the initial invocation of *dev_ultra* or when the state of the machine is unknown. Also, the following invocation sequence should be used if any hard errors have occurred since the last system initialization.

Figure dev_ultra–1, Initial Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
:test dev_ultra [-c [class number(s)]] [-s [subtest number(s)]] [-option] [-f FILE] [+>filename] RETURN
```

In actual usage, all the prompts and responses appear sequentially on the screen, one line at a time. All prompts and responses are shown in one figure for convenience.

> **NOTE**
>
> After entering **dshell**, specific *dshell* parameters may be changed. Refer to the "Dshell Overview" chapter of this manual for more information.

Entering only **test dev_ultra** executes all applicable *dev_ultra* subtests sequentially. To execute a specific class(es) of subtest(s) or one or more individual subtests, use the **-c** or **-s** options during

test invocation, respectively. Detailed information for using these options can be found in the "Dshell Overview" chapter of this manual.

The following list defines the dash options ([-*option*]):

> **NOTE**
>
> In the following list, the **-d, -e, -i, -m,-u, -U,** and **-o** options either override the settings specified in the parameter save file (when the test is invoked with the **-q** option or with the **dev_ultrax** invocation sequence) or the defaults for the prompts in the **Test Parameter Menu**.

-V Print the version (build date, or last modification) of this test

-d *flgs* Set debug flags to *flgs*

-e *act* Set VMEbus UltraNet controller error action to *act*

-F *FILE* Use alternate CCU driver file (*FILE*), default is */mnt/os/viop*, if it exists; if not, default is */mnt/test/dev_ultra.x00*

-f *FILE* Use *FILE* as the parameter save file. If this option is omitted, the parameter file used is */tmp/dev_ultra.tmp*

-i *iter* Set iteration count to *iter*

-m *mode* Set error mode to *mode*

-n Do not actually execute any subtest (used to create a parameter file without actually executing any subtest or display parameter file information with **-q**)

-o *opts* Set external connections to *opts*

-q Quick startup (use previous parameters from last test invocation — same as **dev_ultrax**)

-t Execute all applicable subtests sequentially (override parameter file subtest list)

-u Same as answering **y** to the `Use Controller even if Already Online` prompt

-U Same as answering **n** to the `Use Controller even if Already Online` prompt

-v Set verbose flag (detailed information printed)

The [+>*filename*] option allows the test results to be written to *filename* as well as displayed.

NOTE

The following alternate test invocation procedure is optimal when invoking *dev_ultra* multiple times. Using this invocation sequence insures that the test is invoked and executed with all the setup parameters supplied when the test was last executed with the initial invocation sequence.

Figure dev_ultra–2, Alternate Test Invocation Sequence

```
(spu)> cd /mnt/test RETURN
(spu)> sysreset RETURN
(spu)> mminit -s RETURN
(spu)> dshell RETURN
:test dev_ultrax [-c [class number(s)]] [-s [subtest number(s)]] [-option] [-f FILE] [+>filename] RETURN
```

The only difference in this alternate invocation sequence is the **x** after **dev_ultra**. When invoking *dev_ultra* in this manner, no prompts are displayed. The diagnostic obtains all prompt information from the parameter file created when the initial invocation sequence was performed. Also note that **mminit -s** and **sysreset** are only required if the state of the machine is unknown or if hard errors have occurred since the last system initialization.

Test Parameter Menu

Once the test is invoked, a test menu prompt is presented allowing selection of default switches. The following figure shows all prompts, their possible answers (in brackets [ ]), and their default answers (in parentheses ( )). The prompts and responses appear sequentially on the screen, one line at a time. The figure illustrates *all* questions that can be displayed during test parameter input; however, some questions may be omitted, depending on answers to previous questions. In all cases, questions are numbered sequentially.

Figure dev_ultra–3, Test Parameter Menu

```
                    ENTER TEST PARAMETERS

        []      Encloses allowed input ranges or values
        ()      Encloses the default value
        ^       Returns to the previous prompt
        :nn     Returns to the prompt # nn
        :       Returns to the first unsatisfied prompt
        :?      Reviews previous entries
        ?       Provides specific help where available

 1: Select ioconfig file [<filepath>,?]       (/ioconfig) -> RETURN


      PERIPHERAL CONFIGURATION DATA
     CCU    Chassis   Type    CSR   Int
    -------- ------- -------- ------ ---
 1) viop  3     0    LAN-202  0x7740  3
 2) viop  3     1    LAN-202  0x7740  3

         *** Enter 0 for manual configuration ***

 2: Ioconfig File Unit to Test [1-2,0,?]                  (1) -> 0
 3: VMEbus IOP Number [3-7,?]                             (3) -> RETURN
 4: VMEbus Chassis Number [0-1,?]                         (0) -> RETURN
 5: VMEbus CSR of the Controller [0x0-0xffe0,?]      (0x7740) -> RETURN
 6: VMEbus Interrupt Level of the Controller [1-7,?]      (3) -> RETURN
 7: Use Defaults for Remaining Parameters [y,n,?]          (y) -> n
       ** External Connections (bit mapped) **
    0x0001: Enable External Loopback
    0x0002: Direct Connection to CONVEX Machine

 8: Enable External Loopback [0x0-0x3,?]                (0x0) -> RETURN
 9: Use Controller even if Already Online [y,n,?]          (n) -> RETURN
10: Number of Iterations for Each Subtest [1-2147483647,?]
                                                           (1) -> RETURN
11: Use Defaults for Subqueue Assignments [y,n,?]          (y) -> n
12: SQ_HW_CTL Queue Number [0-7,?]                         (0) -> RETURN
13: SQ_CONTROL Queue Number [0-7,?]                        (1) -> RETURN
14: SQ_URGENT Queue Number [0-7,?]                         (2) -> RETURN
15: SQ_READ Queue Number (not used) [0-7,?]                (3) -> RETURN
16: SQ_WRITE Queue Number (not used) [0-7,?]               (4) -> RETURN
17: SQ_DEVICE Queue Number (not used) [0-7,?]              (5) -> RETURN
18: SQ_DIAG Queue Number [0-7,?]                           (6) -> RETURN
19: SQ_DEBUG Queue Number (not used) [0-7,?]               (7) -> RETURN
```

Figure dev_ultra–3, Test Parameter Menu (continued)

```
        ** Debug Mode Flags (bit mapped) **
    0x0001: Print messages sent to Ultra
    0x0002: Print messages received from Ultra
    0x0004: Pause before message sent to Ultra
    0x0008: Pause after message received from Ultra
    0x0010: Print MBS messages sent to CCU
    0x0020: Print MBS messages received from CCU
    0x0040: Pause before MBS message sent to CCU
    0x0080: Pause after MBS message received from CCU
    0x0100: Print extra informative messages
    0x0200: Don't reset Ultra after subtest is aborted
    0x0400: Don't disable SPU interrupts when done
    0x0800: Simulate all MBS messages (don't send them)

20: Select Debug Mode [0x0-0xfff,?]                    (0x0) -> RETURN

        ** Subtest Error Actions **
    1:  Silently ignore subtest errors
    2:  Pause for subtest errors
    3:  Abort subtest on first error

21: Select Subtest Error Action [1-3,?]                  (2) -> RETURN

        ** Error Start/Finish Text Options (bit mapped) **
    0x0001: Enable error start text
    0x0002: Enable error finish text

22: Select Error Start/Finish Message Mode [0x0-0x3,?]  (0x0) -> 3
23: Error Start Character Sequence [<error start string>,?]
                                                  (\033[?5i) -> RETURN
24: Error Finish Character Sequence [<error finish string>,?]
                                                  (\033[?4i) -> RETURN
25: Enter OK, or :NN to return to question NN [OK]        (OK) -> OK
```

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

For help or information during test parameter entry, enter one of the following characters followed by a RETURN:

Table dev_ultra–2, Getting Help During Test Parameter Entry

Character	Description
:?	Reviews previous entries
?	Provides specific help where available

After the desired help information displays, the system redisplays the last prompt.

When all prompts are answered, the screen displays a TEST PARAMETER SUMMARY that displays the prompts that were answered and their responses. The following figure illustrates an example of a TEST PARAMETER SUMMARY screen. The actual values and responses vary according to the input.

Figure dev_ultra–4, Sample Test Parameter Summary

```
                    TEST PARAMETER SUMMARY

Select ioconfig file                                  : /ioconfig
Ioconfig File Unit to Test                            : 0
VMEbus IOP Number                                     : 3
VMEbus Chassis Number                                 : 0
VMEbus CSR of the Controller                          : 0x7740
VMEbus Interrupt Level of the Controller              : 3
Use Defaults for Remaining Parameters                 : n
Enable External Loopback                              : 0x0000
Use Controller even if Already Online                 : n
Number of Iterations for Each Subtest                 : 1
Use Defaults for Subqueue Assignments                 : n
SQ_HW_CTL Queue Number                                : 0
SQ_CONTROL Queue Number                               : 1
SQ_URGENT Queue Number                                : 2
SQ_READ Queue Number (not used)                       : 3
SQ_WRITE Queue Number (not used)                      : 4
SQ_DEVICE Queue Number (not used)                     : 5
SQ_DIAG Queue Number                                  : 6
SQ_DEBUG Queue Number (not used)                      : 7
Select Debug Mode                                     : 0x0000
Select Subtest Error Action                           : 2
-> Pause for subtest errors <-
Select Error Start/Finish Message Mode                : 0x0003
-> Enable error start text <-
-> Enable error finish text <-
Error Start Character Sequence                        : \033[?5i
Error Finish Character Sequence                       : \033[?4i
Enter OK, or :NN to return to question NN             : OK
```

Initialization Sequence for *dev_ultra*

After the last prompt is entered, and before subtest code execution, the following events occur:

- The diagnostic determines if the test was invoked for quick startup (i.e., **dev_ultrax** or **dev_ultra -q**). If so, the diagnostic reads the test parameters from the specified parameter file (default parameter file is */tmp/dev_ultra.tmp*). If not, the input parameters are written to the parameter file (default or user specified).
- The diagnostic checks to see if the CCU is already loaded with the *dev_ultra* CCU driver. If the driver is not loaded, the CCU is reloaded. After the load completes, the driver is configured for EGOS and then the EGOS probe message starts the driver.

> **NOTE**
>
> The file */mnt/boot_db* is used to determine what memory is installed. If this file is non-existent, it can be created with the command: **scn_util -b > /mnt/boot_db** from the (spu)> prompt.

After all these events have occurred, the test code is started.

Prompt Explanations

The test parameter prompts are repeated and explained in the following paragraphs.

```
1: Select ioconfig file [<filepath>,?]          (/ioconfig) ->
```

This option allows specification of an alternate */ioconfig* file. The file must still be in the same format as a conventional */ioconfig* file.

```
        PERIPHERAL CONFIGURATION DATA
      CCU     Chassis   Type     CSR    Int
    -------- ------- -------- ------ ---
 1) viop  3      0    LAN-202  0x7740  3
 2) viop  3      1    LAN-202  0x7740  3

*** Enter 0 for manual configuration ***

 2: Ioconfig File Unit to Test [1-2,0,?]                    (1) ->
```

Above, the applicable */ioconfig* file entries (if any) are listed . To select a predefined controller configuration entry from the */ioconfig* file, enter the number that is found to the left of the desired entry. Entering a **0** allows each item within the controller configuration entry to be independently specified. If most, but not all, items associated with a given entry in */ioconfig* file are desired, select the number for that entry, back up to this prompt (by entering ^ RETURN), and specify **0** the second time. This causes the default values for the independent items to be the same as the originally selected entry.

```
3: VMEbus IOP Number [3-7,?]                               (3) ->
```

Enter the CCU slot number for the VMEbus IOP that controls the VMEbus chassis containing the UltraNet controller.

```
4: VMEbus Chassis Number [0-1,?]                           (0) ->
```

Enter the VMEbus chassis number for the chassis where the UltraNet controller is installed. If there is only 1 chassis, the number is usually 0.

```
5: VMEbus CSR of the Controller [0x0-0xffe0,?]        (0x7740) ->
```

Enter the VMEbus address of UltraNet Controller Status Register. The standard address for the UltraNet controller is 0x7740.

```
6: VMEbus Interrupt Level of the Controller [1-7,?]        (3) ->
```

Enter the CONVEX VMEbus interrupt number assigned to the UltraNet controller board under test. The interrupt number must be between 1 and 7, inclusive. The standard interrupt number for UltraNet is 3.

```
7: Use Defaults for Remaining Parameters [y,n,?]          (y) ->
```

Enter **y** to select the default values for all remaining prompts. This bypasses entering a RETURN in response to every remaining prompt.

```
    ** External Connections (bit mapped) **
0x0001: Enable External Loopback
0x0002: Direct Connection to CONVEX Machine

8: Enable External Loopback [0x0-0x3,?]                   (0x0) ->
```

Select what external connections, if any, are available for the test. If a loopback jumper is attached to the transceiver, the external data path through the transceiver is tested. If no loopback jumper is present, the UltraNet controller is tested only with an internal loopback path and the transceiver and cables are not tested. Option 0x0002 is ignored at this time.

```
9: Use Controller even if Already Online [y,n,?]          (n) ->
```

Enter **y** to override the exclusive open flag on the VIOP driver. The exclusive open flag is clear if the VIOP was loaded by this test. This option is used for debugging test/driver problems.

```
10: Number of Iterations for Each Subtest [1-2147483647,?]
                                                          (1) ->
```

Enter the number of times each subtest is to be executed on the UltraNet controller. This is most useful for repeating a subtest many times in quick succession. This may also be set using the **-i** command line option during test invocation.

```
11: Use Defaults for Subqueue Assignments [y,n,?]         (y) ->
```

Enter **y** to select the default values for subqueue assignments. Subqueue assignments can be changed to allow this test to work with non-standard VIOP code (i.e., all control queues are mapped into the hardware control queue). The default subqueue assignments are:

SQ_HW_CTL	0	# Hardware control functions
SQ_CONTROL	1	# Software control functions
SQ_URGENT	2	# Software control functions (priority)
SQ_READ	3	# (Not used by the dev_ultra diagnostic)
SQ_WRITE	4	# (Not used by the dev_ultra diagnostic)
SQ_DEVICE	5	# (Not used by the dev_ultra diagnostic)
SQ_DIAG	6	# Diagnostic tests
SQ_DEBUG	7	# (Not used by the dev_ultra diagnostic)

```
12: SQ_HW_CTL Queue Number [0-7,?]                        (0) ->
```

Refer to the explanation of the **Use Defaults for Subqueue Assignments** prompt (number 11 in this test description) for information on default values for subqueue assignments.

```
13: SQ_CONTROL Queue Number [0-7,?]                       (1) ->
```

Refer to the explanation of the **Use Defaults for Subqueue Assignments** prompt (number 11 in this test description) for information on default values for subqueue assignments.

```
14: SQ_URGENT Queue Number [0-7,?]                    (2) ->
```

Refer to the explanation of the **Use Defaults for Subqueue Assignments** prompt (number 11 in this test description) for information on default values for subqueue assignments.

```
15: SQ_READ Queue Number (not used) [0-7,?]           (3) ->
```

Refer to the explanation of the **Use Defaults for Subqueue Assignments** prompt (number 11 in this test description) for information on default values for subqueue assignments.

```
16: SQ_WRITE Queue Number (not used) [0-7,?]          (4) ->
```

Refer to the explanation of the **Use Defaults for Subqueue Assignments** prompt (number 11 in this test description) for information on default values for subqueue assignments.

```
17: SQ_DEVICE Queue Number (not used) [0-7,?]         (5) ->
```

Refer to the explanation of the **Use Defaults for Subqueue Assignments** prompt (number 11 in this test description) for information on default values for subqueue assignments.

```
18: SQ_DIAG Queue Number [0-7,?]                      (6) ->
```

Refer to the explanation of the **Use Defaults for Subqueue Assignments** prompt (number 11 in this test description) for information on default values for subqueue assignments.

```
19: SQ_DEBUG Queue Number (not used) [0-7,?]          (7) ->
```

Refer to the explanation of the **Use Defaults for Subqueue Assignments** prompt (number 11 in this test description) for information on default values for subqueue assignments.

```
    ** Debug Mode Flags (bit mapped) **
0x0001: Print messages sent to Ultra
0x0002: Print messages received from Ultra
0x0004: Pause before message sent to Ultra
0x0008: Pause after message received from Ultra
0x0010: Print MBS messages sent to CCU
0x0020: Print MBS messages received from CCU
0x0040: Pause before MBS message sent to CCU
0x0080: Pause after MBS message received from CCU
0x0100: Print extra informative messages
0x0200: Don't reset Ultra after subtest is aborted
0x0400: Don't disable SPU interrupts when done
0x0800: Simulate all MBS messages (don't send them)
20: Select Debug Mode [0x0-0xfff,?]                   (0x0) -> ?
```

These options allow the standard test behavior to be altered in ways that are often useful for troubleshooting. In addition, the test can be paused before and after (or both) each command (i.e., typically one controller operation) is sent to the CCU driver. These flags may also be set using the **-v** and **-d** command line options during test invocation. The first four flags (0x0001–0x0008) control printing of all messages that are sent to the VMEbus UltraNet controller. The next four flags (0x0010–0x0080) independently control printing (before or after) of messages that are sent to the CCU. If the flag 0x0100 is set, verbose messages are printed just as if the **-v** option had been set from the command line. If the flag 0x0200 is set, the controller is not reset after a subtest is aborted (used for debugging). If the flag 0x0400 is set, the SPU interrupts, MBS message interrupt, and CCU printer interrupt are not disabled when the diagnostic is

completed. If flag 0x0800 is set, a simulation of the test is done without affecting the CCU or the controller.

```
    ** Subtest Error Actions **
1:  Silently ignore subtest errors
2:  Pause for subtest errors
3:  Abort subtest on first error

21: Select Subtest Error Action [1-3,?]                    (2) -> ?
```

Enter the desired subtest error action.

1. Ignores all errors (as if they never happened). This could be useful when it is necessary to just generate constant action (for example, an EMI test).
2. Passes all errors to the *dshell* for processing. Choose this option for running the test normally [default].
3. Causes the subtest to abort when the first error is seen, regardless of any *dshell* error actions specified.

```
22: Select Error Start/Finish Message Mode [0x0-0x3,?]  (0x0) ->
```

This prompt allows a specified character string to be sent to the printer before and after (or both) an error (and its data) is displayed. Although any string up to 64 characters in length may be specified, the intended use is to selectively turn a printer on before an error is displayed and to turn a printer off after an error has been displayed. This is a paper saving feature when running the diagnostic multiple times or for long periods of time. This assumes a printer is connected to the auxiliary port on the display terminal where the diagnostic is running. It also assumes the auxiliary port can be turned on and off via an escape character sequence.

Selection of both options is achieved by entering the hexadecimal mask obtained by ORing the two options together (0x03). Control characters may be specified by using standard "C" programming style escape sequences. For example:

\033	Octal value of the ASCII escape character (0x1b)
\x1b	Same as above value but specified in hex
\r	Carriage return
\n	Line feed
\t	Tab character
\b	Backspace character
\f	Form feed character
\a	Bell ("alert") character
\v	Reverse line feed character

```
23: Error Start Character Sequence [<error start string>,?]
                                                    (\033[?5i) ->
```

Enter the string to be displayed before showing an error message. The default value is the "Enter Auto Print Mode" sequence for terminals that support VT100 terminal protocol.

Control characters may be specified by using standard "C" programming style escape sequences. For example:

\033	Octal value of the ASCII escape character (0x1b)
\x1b	Same as above value but specified in hex
\r	Carriage return
\n	Line feed
\t	Tab character
\b	Backspace character
\f	Form feed character
\a	Bell ("alert") character
\v	Reverse line feed character

```
24: Error Finish Character Sequence [<error finish string>,?]
                                                    (\033[?4i) ->
```

Enter the string to be displayed after showing an error message. The default value is the "Exit Auto Print Mode" sequence for terminals that support VT100 terminal protocol.

Control characters may be specified by using standard "C" programming style escape sequences. For example:

\033	Octal value of the ASCII escape character (0x1b)
\x1b	Same as above value but specified in hex
\r	Carriage return
\n	Line feed
\t	Tab character
\b	Backspace character
\f	Form feed character
\a	Bell ("alert") character
\v	Reverse line feed character

```
25: Enter OK, or :NN to return to question NN [OK]        (OK) -> OK
```

If **OK** or RETURN is entered, the test parameter menu terminates and all inputs are no longer changeable.

Class Descriptions

The *dev_ultra* test contains the three classes of subtests as listed in the following table:

Table dev_ultra–3, *dev_ultra* Test Classes

CLASS	DESCRIPTION
1	VMEbus UltraNet Controller Test
2	VMEbus UltraNet Controller Extended Tests
3	VMEbus UltraNet Controller Addressing Test

All subtests contained in *dev_ultra* may be looped under the *dshell*.

Class 1 Subtest

Class 1 contains only one subtest. The following table lists the Class 1 subtest, its description, and the time required to execute the subtest:

Table dev_ultra–4, Class 1 Subtest

Subtest	Description	Time (minsec)
100	VMEbus UltraNet Controller Reset Test	00:01

Subtest 100, VMEbus UltraNet Controller Reset Test

Subtest 100 verifies access to the VMEbus UltraNet controller and reports the results of the controller's most recent power-on reset test. The subtest verifies the following:

- The ability to communicate with the VMEbus Input/Output Processor (VIOP), VMEbus Control Unit (VBCU), and the VMEbus UltraNet controller.
- The ability of the VMEbus UltraNet controller to interrupt the VIOP.

The information from the power-on test varies with the version of the VMEbus UltraNet controller EPROM code. If the EPROM code version is less than five, the only information available is the EPROM version and the results of the power-on test. For EPROM code versions greater than or equal to five, the hardware model, version, revision, options, and serial number are shown.

Class 2 Subtests

Class 2 contains two subtests. The following table lists the Class 2 subtests, their descriptions, and the times required to execute each subtest:

Table dev_ultra–5, Class 2 Subtests

Subtest	Description	Time (min:sec)
200	EPROM-based Test (Internal Loopback)	00:04
201	EPROM-based Test (External Loopback)	00:04

Subtest 200, VMEbus UltraNet Controller EPROM-based Test (Internal Loopback)

Subtest 200 tests all major functional units of the VMEbus UltraNet controller. The testing sequence is:

- Check EPROM checksum
- Test controller RAM—the RAM test consists of pattern-testing the RAM with 8-bit, 16-bit, and 32-bit accesses
- Check Programmable Interrupt Controller (PIC) and Programmable Interval Timer (PIT)
- Verify that internal loopback is functioning
- Check FIFO RAM with 80386 processor accesses
- Test Checksum Gate Arrays (used to compute checksums on data packets)
- Test controller interrupt processing
- Test VMEbus memory access—the VMEbus RAM is tested with a pattern test
- Test FIFO RAM with DMA accesses

Subtest 201, VMEbus UltraNet Controller EPROM-based Test (External Loopback)

Subtest 201 tests all major functional units of the VMEbus UltraNet controller. The FIFO tests use an external loopback path that goes through the external transceiver and loopback cable (Part Number TBD). If the loopback cable is not installed, this test is not executed. However, if two CONVEX machines are directly connected via VMEbus UltraNet controllers, the subtest can be fully exercised by following these steps:

1. Execute the *dev_ultra* diagnostic from both machines (does not have to be concurrently) with the **-s 200** option.
2. Execute the *dev_ultra* diagnostic from one machine with the **-s 201** option and the **-o 3** option.

The Subtest 201 testing sequence is:

- Check EPROM checksum
- Test controller RAM—the RAM test consists of pattern-testing the RAM with 8-bit, 16-bit, and 32-bit accesses
- Check Programmable Interrupt Controller (PIC) and Programmable Interval Timer (PIT)
- Verify that external loopback is functioning
- Check FIFO RAM with 80386 processor accesses
- Test Checksum Gate Arrays (used to compute checksums on data packets)
- Test controller interrupt processing
- Test VMEbus memory access—the VMEbus RAM is tested with a pattern test
- Test FIFO RAM with DMA accesses

Class 3 Subtests

Class 3 contains only one subtest. The following table lists the Class 3 subtest, its description, and the time required to execute the subtest:

Table dev_ultra–6, Class 3 Subtest

Subtest	Description	Time (min:sec)
300	VMEbus UltraNet Controller Addressing Test	00:01

Subtest 300, VMEbus UltraNet Controller Addressing Test

Subtest 300 tests the ability of the VMEbus UltraNet controller to address all available addresses in VMEbus address space. The controller reads data from each page of VMEbus memory and writes a reply back to the address. This subtest must have complete control of the VIOP, as it temporarily disables MBS and EGOS interrupts while changing the VMEbus cache controller page maps.

Error Messages

There are two basic types of error messages associated with this diagnostic:

- Error messages associated with the diagnostic's start-up
- Error messages associated with the execution of the diagnostic's subtests

Start-up Error Messages

The first type of error messages are errors reported during the start-up sequence of the diagnostic. These messages do not contain header and footer information. They consist of a start-up error message and, when long messages are enabled from *dshell*, a secondary subtest error message may also occur. When the verbose bit is set and long messages are enabled from *dshell*, a source file information message is also provided.

The following start-up error messages may occur:

```
CMI command returned fail status (0x17)

File is not in b.out format (0x07)

File not found (0x0A)

Invalid command (0x10)

MBS error occurred (0x09)

Subtest aborted by operator (0x21)

Subtest failed (0x20)

Timeout waiting for CCU driver reply (0x08)

Timeout waiting for Ultra reply (0x12)

Ultra is owned by another process (0x13)

Ultra not initialized (0x11)

Unable to allocate CCU windows for message (0x14)

Unable to allocate main memory (0x16)

Unable to configure LAN-202 driver (0x05)

Unable to initialize CCU (0x04)

Unable to initialize processor queues (0x01)

Unable to probe LAN-202 driver (0x06)
```

Subtest Error Messages

The second type of error messages are errors reported by an executing subtest (i.e., subtest failures). These messages contain a standard header and footer, subtest error message, and the following information:.

- Iteration—lists which iteration of the subtest was being executed at the time of the failure
- Reason(s)—describes the error condition and usually contains actual and expected values

The following figure contains an example of the standard header message:

Figure dev_ultra–5, Standard Header for Error Messages

```
*****  Thu Nov  9 15:46:48 CST 1989  *****
Test:    dev_ultra.t 1.2   Class: 1    Subtest: 100 1.1   Count: 1    Error: 0
Failed:  VMEbus UltraNet Controller Reset Test
```

The following figure contains an example of a standard footer that is printed after the standard header and error message:

Figure dev_ultra–6, Standard Footer for Error Messages

```
Test 'dev_ultra.t' failed
Elapsed time:   0:00:03
```

The following list contains all possible reasons that could be listed in the subtest error message:

```
Reason(s): Unable to initialize processor queues

Reason(s): Unable to initialize CCU

Reason(s): Unable to configure LAN-202 driver

Reason(s): Unable to probe LAN-202 driver

Reason(s): File is not in b.out format

Reason(s): Timeout waiting for CCU driver reply

Reason(s): MBS error occurred
```

```
Reason(s): File not found
Reason(s): Invalid command
Reason(s): Ultra not initialized
Reason(s): Timeout waiting for Ultra reply
Reason(s): Ultra is owned by another process
Reason(s): Unable to allocate CCU windows for message
Reason(s): Unable to allocate main memory
Reason(s): CMI command returned fail status
Reason(s): Subtest failed
Reason(s): Subtest aborted by operator
Reason(s): Unknown cmi status: 0xXX
Reason(s): Non-specific error status
Reason(s): Device driver not found
Reason(s): Device not found
Reason(s): Unit not found
Reason(s): Unit already connected
Reason(s): Unit disconnected
Reason(s): Unit already online
Reason(s): Unit offline
Reason(s): Unit already mounted
Reason(s): Unit not mounted
Reason(s): No memory for initialization
Reason(s): Out of CCU windows
Reason(s): Function timeout exceeded
Reason(s): Function aborted by CCU
Reason(s): Invalid CMI function code
Reason(s): Dev_name value is unsupported
Reason(s): Unit_name value is unsupported
Reason(s): Dev_class value is unsupported
```

```
Reason(s) : Dev_type value is unsupported
Reason(s) : CMI revision unsupported by CCU
Reason(s) : Defective CMI message (bad parameters)
Reason(s) : CMI message is required (not MBS)
Reason(s) : Controller already initialized
Reason(s) : Controller not initialized
Reason(s) : Unable to initialize device queues
Reason(s) : Hardware failure on controller
Reason(s) : Bad sequence number on firmware load record
Reason(s) : Option only valid on first record
Reason(s) : Option only valid on last record
Reason(s) : Unable to start firmware
Reason(s) : Unable to load firmware record
Reason(s) : Memory allocation failed
Reason(s) : Attempt to write on write protected unit
Reason(s) : Retries were required to complete command
Reason(s) : Unit is not ready
Reason(s) : Could not seek to required location
Reason(s) : Unrecoverable error even with ECC
Reason(s) : Bad header (checksum failed)
Reason(s) : Operation would run beyond last block
Reason(s) : Function canceled by CPU
Reason(s) : Device address not valid
Reason(s) : Bad parity or non-existent memory
Reason(s) : Unrecoverable memory error
Reason(s) : CCU-detectable physical I/O error
Reason(s) : Function invalid for subqueue
Reason(s) : Read/write data request too large
Reason(s) : Requested data not available
```

```
Reason(s) : Dev_type does not match installed hardware

Reason(s) : MBS error detected by CCU

Reason(s) : No MBS message

Reason(s) : Too many drivers in /ioconfig file

Reason(s) : CCU driver didn't return a status code

Reason(s) : Diagnostic test failed
            Error(s) reported by UltraNet self-test:
            No errors returned by UltraNet self-test
            EPROM checksum incorrect
            RAM check failed
            Interrupt Controller or Interval Timer failed
            Loopback connector check failed
            FIFO memory test failed
            Checksum PAL test failed
            Non-Maskable Interrupt control test failed
            VMEbus Memory test failed
            FIFO memory/DMA test failed
            FIFO control test failed
            Address check test failed:
            Expected address: XXXXXX
            Actual address:   YYYYYY
            Address check test passed
            Unknown command (0xXXXX)

Reason(s) : No errors returned by UltraNet self-test

Reason(s) : Error(s) reported by UltraNet self-test:
            EPROM checksum incorrect
            RAM check failed
            Interrupt Controller or Interval Timer failed
            Loopback connector check failed
            FIFO memory test failed
            Checksum PAL test failed
            Non-Maskable Interrupt control test failed
            VMEbus Memory test failed
            FIFO memory/DMA test failed
            FIFO control test failed

Reason(s) : Address check test failed:
            Expected address: XXXXXX
            Actual address:   YYYYYY

Reason(s) : Address check test passed

Reason(s) : Unknown command (0xXXXX)
```

Appendix A
Reporting Problems

A.1 Overview

This appendix introduces the CONVEX Technical Assistance Center (TAC) and the *contact* utility. The *contact* utility is an online system for reporting problems to the TAC. To learn *contact* by using it, enter **contact** at the system prompt and then answer the questions as they appear on the screen. To find out more about using *contact*, read through this appendix. It describes prerequisites and tips for using *contact* and the step-by-step process *contact* takes you through.

A.2 Technical Assistance Center

The CONVEX Technical Assistance Center (TAC) is staffed by technical specialists who can address the diverse questions and problems that arise in a supercomputing environment. If you have a hardware, software, or documentation problem, contact the TAC. This group stands ready to solve such problems.

A.3 The *contact* Utility

The TAC recommends using the *contact* utility to report a hardware, software, or documentation problem. The *contact* utility is an interactive utility that helps the TAC track reports and route them to the the CONVEX personnel most qualified to fix them.

After invoking *contact*, it prompts for information about the problem. When you finish your report, *contact* electronically mails it to the TAC. You are notified within 48 hours that the TAC has received your report.

A.4 Prerequisites

To use *contact* requires

- a UNIX-to-UNIX Communication Protocol (UUCP) connection to the TAC
- the full path name of the program or utility in question
- the version number of the program or utility in question

A.4.1 UUCP Connection

Before using *contact*, check with your system administrator to be sure there is a UUCP connection to the TAC. A UUCP connection allows files to be copied from one UNIX system to another. The *uucp* (UNIX-to-UNIX copy) command relies on either a dial-up or hard-wired UUCP communication line.

A.4.2 Finding the Program Path Name

To determine the full path name of the program or utility in question, use the *which* command. The following screen illustrates using the *which* command to find the full path name of the loader (*ld*) utility:

```
>which ld
/bin/ld
>
```

In this example, the full path name of the loader is */bin/ld*.

For more information on the *which* command, refer to the *which*(1) man page. You can also use the *info* online information system. Enter **info which** at the system prompt. If you use the C shell (*csh*), you can also use the *whence* command to find the program path name. The *whence* command works like *which*, only faster.

A.4.3 Finding the Program Version Number

To determine the version number of the program or utility in question, use the *vers* command. The following screen illustrates using the *vers* command (enter **vers**, then the path name of the program or utility) to find the version number of the loader (*ld*) utility.

```
>vers /bin/ld
/bin/ld: 7.0
>
```

In this example, the loader utility version number is 7.0.

For more information on the *vers* command, refer to the *vers*(1) man page. You can also use the *info* online information system. To do so, enter **info vers** at the system prompt.

A.5 Tips on Using the *contact* Utility

The *contact* utility is interactive and easy to use. This section lists tips to help use it efficiently. In particular, this section tells how to

- use a *.contact* file
- abort a contact session
- resubmit an aborted report
- suspend a contact session
- move from one prompt to another
- use tilde-escape sequences in the *contact* utility

A.5.1 Using a *.contact* File

When invoked, *contact* prompts for information regarding the problem. The first prompt is for your name, title, phone number, and company name. You can, however, create a *.contact* file to skip this first prompt. Follow these steps:

1. Create a *.contact* file in your home directory.
2. Enter your name, job title, phone number, and company name, each on a new line.

When you invoke *contact*, it automatically includes the *.contact* file as input for the first prompt and proceeds to the next prompt.

A.5.2 Aborting the Report

To abort a contact report, either enter the interrupt key (usually CTRL-C) or choose the abort option when prompted by the *contact* utility. Using CTRL-C to abort does not save the contents of the report. Using the abort option saves the contents of the report in a file named *dead.report* in your home directory.

A.5.3 Submitting the *dead.report* File

When aborting a contact session, the *contact* utility saves the report in a file named *dead.report* in your home directory. Using the *contact* command with the *-r* option automatically merges the contents of the *dead.report* file into the new contact session. Enter

contact -r

and *contact* finds the *dead.report* file in your home directory and merges it into the contact report. You can then edit the report. When you end the editing session, *contact* returns to the final prompt, which asks you to review, edit, submit, or abort the report.

A.5.4 Suspending a Report

Sometimes it is necessary to stop in the middle of a contact report and return to the shell (for instance, to suspend the contact session to find the program path name or version number). To suspend the contact session, press CTRL-Z. To return to the contact session, enter **fg**. Using CTRL-Z and the *fg* (foreground) command lets you switch back and forth between the *contact* utility and the shell. You cannot, however, use CTRL-Z and *fg* to switch back and forth if you are using a Bourne shell (*sh*).

A.5.5 Ending a Response

The *contact* utility prompts for information pertinent to your hardware, software, or documentation question. Some prompts require one-line responses; to move to the next prompt, press RETURN. Other prompts require more than a one-line response; to move to the next prompt, press CTRL-D.

A.5.6 Tilde-Escape Sequences

The *contact* utility treats input beginning with a tilde (~) as a special sequence. The character following the tilde is considered a request for a special function. The following tilde sequences are recognized by *contact*:

~e	Start the text editor (defined in your EDITOR environment variable).
~h	Display a list of available tilde-escape sequences.
~p	Print the contact report to the terminal screen.
~r *filename*	Read the contents of *filename* as a response to the current prompt. Some prompts require only a one-line response. This tilde-escape sequence only works for prompts that allow more a than one-line response.
~~	Insert a single tilde as the first character in the line.

A.6 Using the *contact* Utility

The *contact* utility prompts for the following information:

- your name, title, phone number, and corporate name
- the name and version of the product involved
- a one-line summary of the problem
- a detailed description of the problem
- the priority of the problem
- instructions on how to reproduce the problem
- comments about the problem
- comments about the documentation supporting the problem
- files to include in the contact report

The following is a step-by-step discussion of these prompts:

1a. To invoke the *contact* utility, enter **contact** at the system prompt. The system responds with a welcome message and a series of questions regarding your hardware, software, or documentation question. The following screen illustrates the *contact* command and the system response:

```
>contact
Welcome to contact version 0.11 ()

Enter your name, title, phone number, and corporate name (^D to terminate)
>
```

1b. If there is a *.contact* file in your home directory, *contact* skips the first prompt. The following screen illustrates the *contact* command and the system response when a *.contact* file is in your home directory:

```
>contact
Welcome to contact version 0.11 ()

Enter the name of the product involved
>
```

2. The *contact* utility prompts for the version number of the product. If you do not know the version number, use CTRL-Z to suspend the session. Use the *which* (or *whence* if using *csh*) and *vers* commands to find the version number of the product. Use the *fg* command to return to the session and enter the version number in the form X.X or X.X.X.X.
3. The *contact* utility prompts for a one-line summary of the problem. This summary is the subject header in any further correspondence regarding the problem. Make this summary as descriptive as possible in one line.
4. The *contact* utility prompts for a detailed description of the problem. Make this description as complete as possible. Include source code and a stack backtrace whenever possible. (Refer to the *adb*(1) or *csd*(1) man page for information on obtaining a stack backtrace.) The more information provided, the quicker the TAC can isolate and solve the problem.
5. The *contact* utility prompts for the priority of the problem. The following screen illustrates this prompt and the priority levels from which to choose; you must enter a priority number.

```
Enter a problem priority, based on the following:
1) Critical    - work cannot proceed until the problem is resolved.
2) Serious     - work can proceed around the problem, with difficulty.
3) Necessary   - problem has to be fixed.
4) Annoying    - problem is bothersome.
5) Enhancement - requested enhancement.
6) Informative - for informational purposes only.
>
```

6. The *contact* utility prompts for an explanation of how to reproduce the problem. Include the command syntax and options you used and anything else you did to make your program run.
7. The *contact* utility prompts for any other pertinent comments. Include any relevant information.
8. The *contact* utility prompts for suggestions regarding the documentation supporting the product. Indicate if the documentation could be revised to address the question.
9. The *contact* utility asks for the names of files necessary to reproduce the problem. The following screen illustrates the *contact* prompt and sample user response:

```
Are there any files that should be included in this report (yes | no)?
>yes
Please enter the names of the files, one to a line (^D to terminate)
>test.f
>~/subroutines/sub.f
>
```

NOTE

Tilde-escape sequences are not recognized in responses to this prompt. Instead, *contact* treats a tilde in this section to mean your home directory. This convention is based on use of the tilde for expanding file names in *csh*.

If the files specified are small text files, they are automatically included in the contact report. If the files are too big to be included in this report, *contact* gives further instructions on how to submit these files.

To specify a directory, combine the directory files into a single file using the *tar* command (refer to the *tar*(1) man page for further information) or enter each file name in the directory on a single line in the contact report.

10. The *contact* utility prompts you to review, edit, submit, or abort the contact report. The following screen illustrates this prompt:

```
Please select one of the following options:
1) Review the problem report.
2) Edit the problem report.
3) Submit the problem report.
4) Abort the problem report.
>
```

Choose the number of the option you want to select. These options let you do the following:

Review — Review the text of your contact report. You are then prompted again to select an option.

Edit — Edit the text of the contact report. If you choose to edit the report, *contact* puts you in your default text editor.

Submit — Send the report to the CONVEX TAC. You are notified within 48 hours that the TAC has received the report. This option exits the *contact* utility and returns you to the shell environment.

Abort — Save the text of your report in a file named *dead.report* in your home directory. This option exits the *contact* utility and returns you to the shell environment.

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